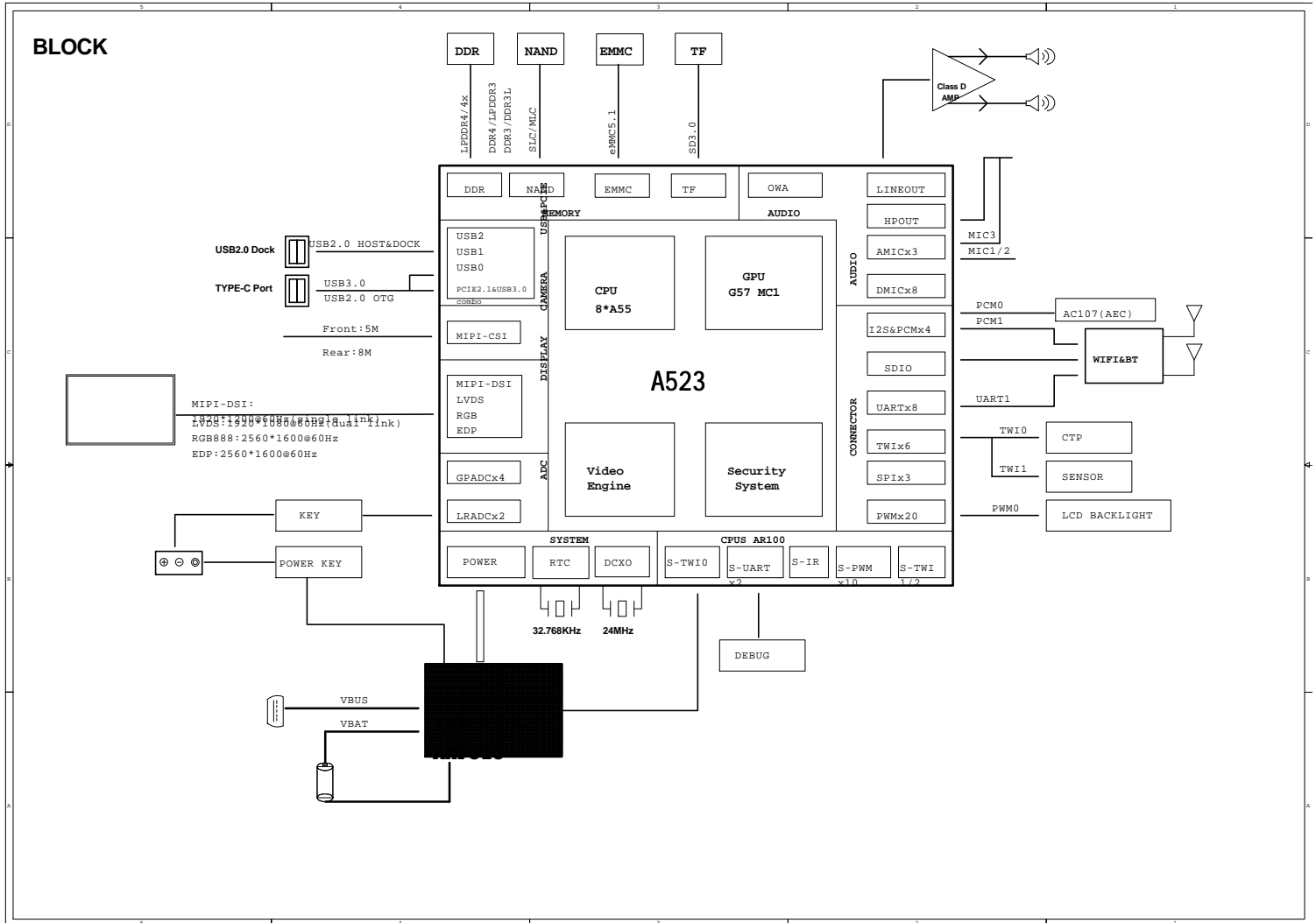


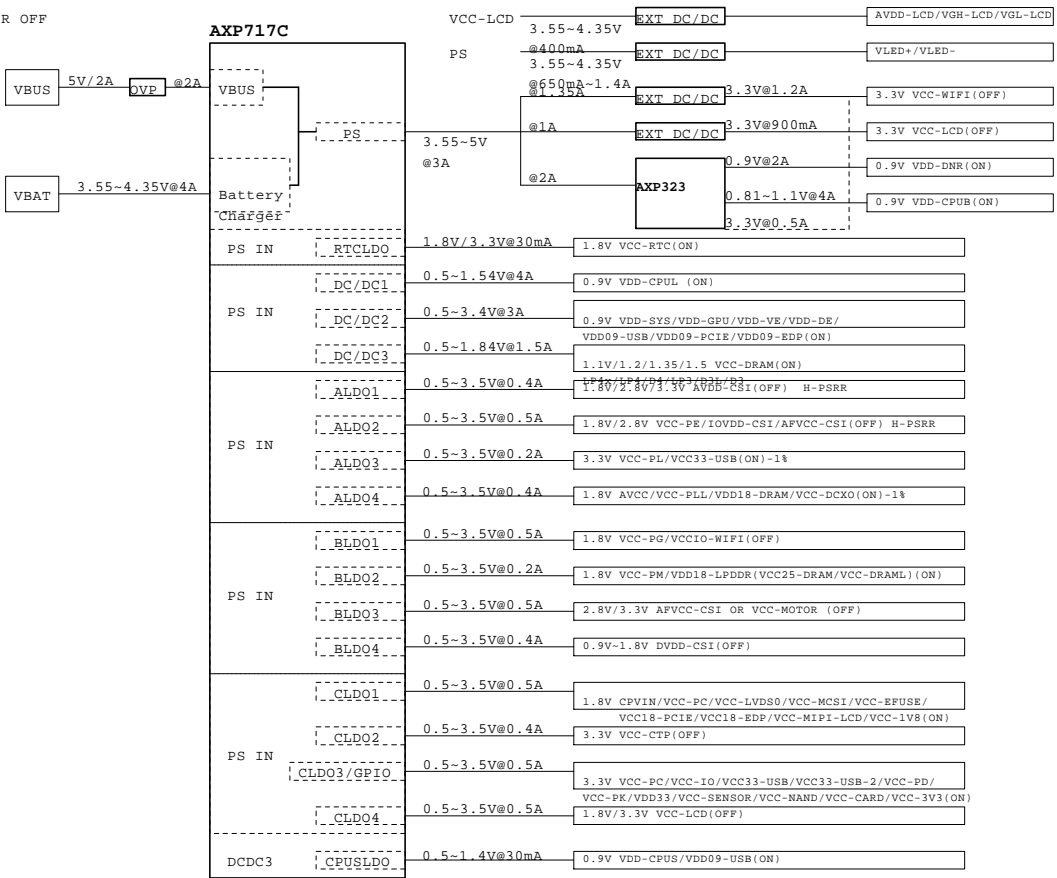
BLOCK



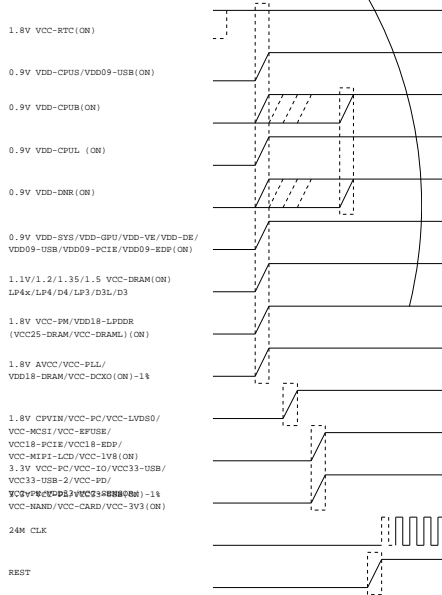
- DEFAULT POWER ON
- DEFAULT POWER OFF

POWER TREE

AXP717C



POWER SEQUENCE



AllWinner Technology Co., Ltd			
AS23-STD-AP717C-AP723-LPDDR4-4K			
D4 POWER SEQUENCE			
Rev	Version	Date	Page
1.0	1.0	2023-12-13	1/1

GPIO ASSIGNMENT

PIN	Define	CFG	Function
PB0	CPUX-TMS	4	DEBUG
PB1	CPUX-TCK	4	
PB2	CPUX-TDO	4	
PB3	CPUX-TDI	4	
PB4	I2S0-MCLK	3	I2S
PB5	I2S0-BCLK	3	
PB6	I2S0-LRCK	3	
PB7			
PB8	I2S0-DIN	3	
PB9	CPUX-TX	2	DEBUG
PB10	CPUX-RX	2	
PB11			
PB12			
PB13			
PB14			

PIN	Define	CFG	Function
PC0	SDC2-DS	3	eMMC
PC1	SDC2-RST	3	
PC2			
PC3			
PC4			
PC5	SDC2-CLK	3	
PC6	SDC2-CMD	3	
PC7			
PC8	SDC2-D3	3	
PC9	SDC2-D4	3	
PC10	SDC2-D0	3	
PC11	SDC2-D5	3	
PC12			
PC13	SDC2-D1	3	
PC14	SDC2-D6	3	
PC15	SDC2-D2	3	
PC16	SDC2-D7	3	

PIN	Define	CFG	Function
PF0	SDC0-D1	2	CARD
PF1	SDC0-D0	2	
PF2	SDC0-CLK	2	
PF3	SDC0-CMD	2	
PF4	SDC0-D3	2	
PF5	SDC0-D2	2	
PF6	SDC0-DET	0	

PIN	Define	CFG	Function
PD0			LCD
PD1			
PD2			
PD3			
PD4			
PD5			
PD6			
PD7			
PD8			
PD9			
PD10	MIPI-DSI1-DP0	4	
PD11	MIPI-DSI1-DN0	4	
PD12	MIPI-DSI1-DP1	4	
PD13	MIPI-DSI1-DN1	4	
PD14	MIPI-DSI1-CKP	4	
PD15	MIPI-DSI1-CKN	4	
PD16	MIPI-DSI1-DP2	4	
PD17	MIPI-DSI1-DN2	4	
PD18	MIPI-DSI1-DP3	4	
PD19	MIPI-DSI1-DN3	4	
PD20			
PD21			
PD22	LCD-RST	1	
PD23	LCD-PWM	3	

PIN	Define	CFG	Function
PG0	WL-SDIO-CLK	2	WIFI/BT
PG1	WL-SDIO-CMD	2	
PG2	WL-SDIO-D0	2	
PG3	WL-SDIO-D1	2	
PG4	WL-SDIO-D2	2	
PG5	WL-SDIO-D3	2	
PG6	BT-UART-RX	2	
PG7	BT-UART-TX	2	
PG8	BT-UART-CTS	2	
PG9	BT-UART-RTS	2	
PG10			
PG11	BT-PCM-CLK	3	
PG12	BT-PCM-SYNC	3	
PG13	BT-PCM-DIN	3	
PG14	BT-PCM-DOUT	3	

PIN	Define	CFG	Function
PM0	WL-WAKE-AP	0	WIFI/BT
PM1	WL-REG-ON	1	
PM2	BT-RESETN	1	
PM3	AP-WAKE-BT	1	
PM4	BT-WAKE-AP	0	
PM5	WL-DIS-N	1	

PIN	Define	CFG	Function
PH0	TWI0-SCK	2	TWI
PH1	TWI0-SDA	2	
PH2	TWI1-SCK	2	
PH3	TWI1-SDA	2	GPIO
PH4	PS-EINT	14	
PH5	OVP-ACOK	0	
PH6	PA-SHDN	1	
PH7	GMA340-SEL	1	
PH8	GMA340-OE	1	
PH9	CTP-INT	14	
PH10	CTP-RST	1	
PH11	GS-INT	14	
PH12	TWI3-SCK	3	
PH13	TWI3-SDA	3	
PH14	3V3-1V8-EN	1	
PH15			
PH16			
PH17	DDR-PARA-SEL-GPIO	0	
PH18	LCD-BL-EN	1	
PH19			

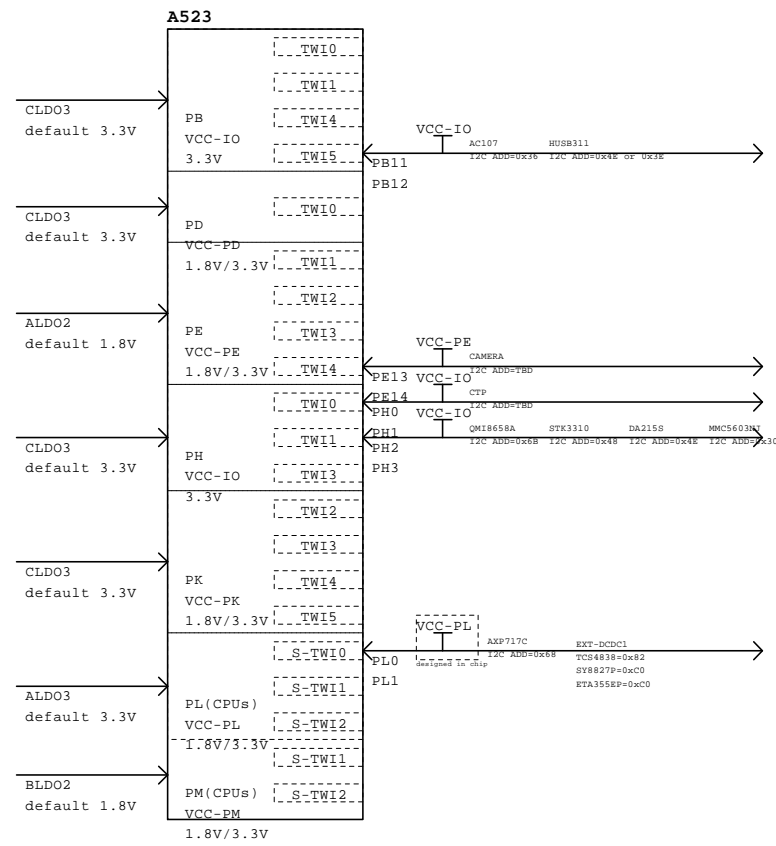
PIN	Define	CFG	Function
PL0	PMU-SCK	2	CPUS
PL1	PMU-SDA	2	
PL2	USB-VBUSDET	0	
PL3	ACIN-DET	0	
PL4	JSB0-EN	1	
PL5	GYRO-INT1	14	
PL6	GYRO-INT2	14	
PL7	VCC-WIFI-PWREN	1	
PL8	JSB1-DRVVBUS	1	
PL9	EINT-HAL	14	
PL10	KD-EINT	14	
PL11	LED-EN	1	
PL12	JSB-DRVVBUS	1	
PL13	CC-INT	14	

PIN	Define	CFG	Function
PK0	MCSIA-D0N	2	MIPI-CSI
PK1	MCSIA-D0P	2	
PK2	MCSIA-D1N	2	
PK3	MCSIA-D1P	2	
PK4	MCSIA-CKN	2	
PK5	MCSIA-CKP	2	
PK6	MCSIB-D0N	2	
PK7	MCSIB-D0P	2	
PK8	MCSIB-D1N	2	
PK9	MCSIB-D1P	2	
PK10			
PK11			
PK12	MCSIC-D0N	2	
PK13	MCSIC-D0P	2	
PK14	MCSIC-D1N	2	
PK15	MCSIC-D1P	2	
PK16	MCSIC-CKN	2	
PK17	MCSIC-CKP	2	
PK18			
PK19			
PK20			
PK21			
PK22			
PK23			

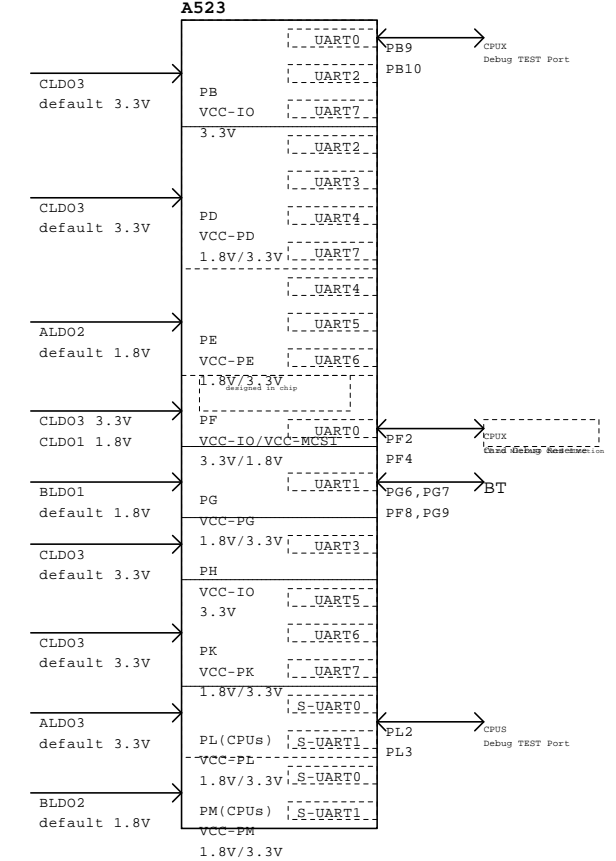
PIN	Define	CFG	Function
PE0			CAMERA
PE1			
PE2			
PE3			
PE4			
PE5			
PE6	MCSIB-STBY-F	1	
PE7	MCSIB-RST-F	1	
PE8	MCSIA-STBY-R	1	
PE9	MCSIA-RST-R	1	
PE10			
PE11			
PE12			
PE13	MCSI-SCK	2	
PE14	MCSI-SDA	2	
PE15	MCSI-MCLK	2	

AllWinner Technology Co., Ltd			
Design Name: A523-STD-AXP717C-AXP323-LPDDR4-4X			
Size	Page Name	Rev	
4	05 GPIO ASSIGNMENT	7	
Date	Wednesday, December 13, 2023		Sheet 5 of 25

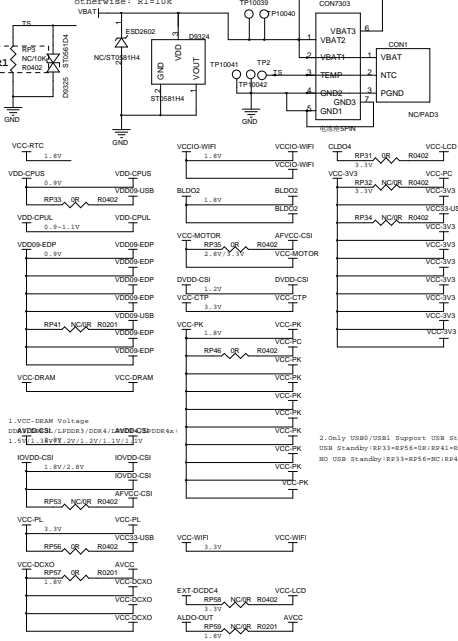
TWI MAP



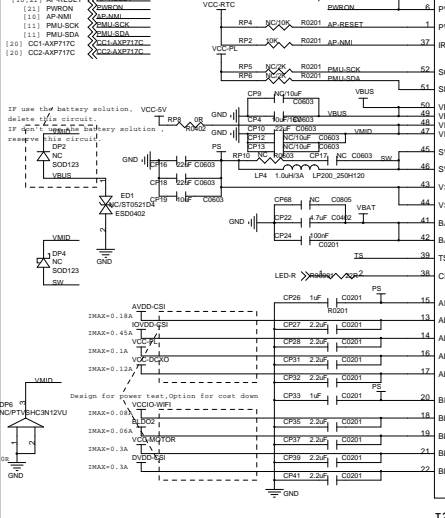
UART MAP



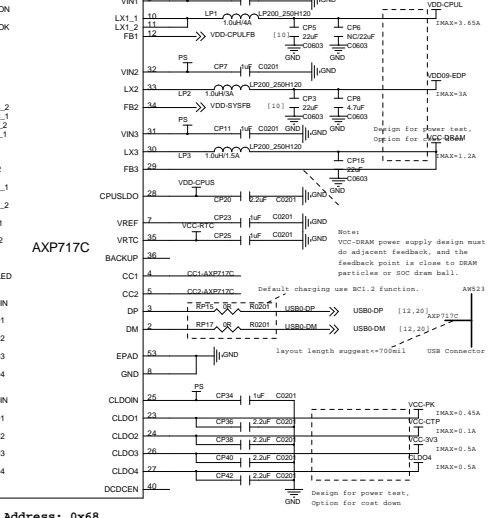
BAT



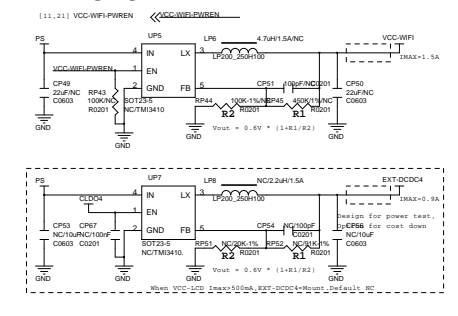
PMIC



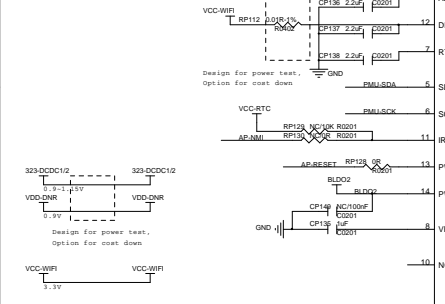
AXP171C



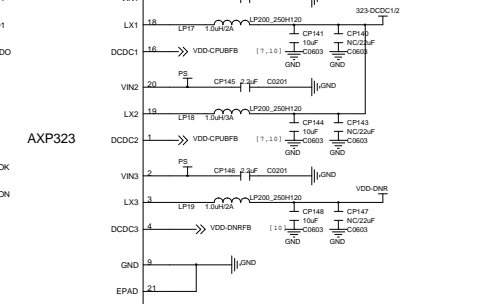
EXT DCDC Design for WIFI SDIO3.0



AXP323



AXP323



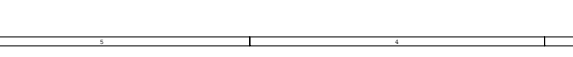
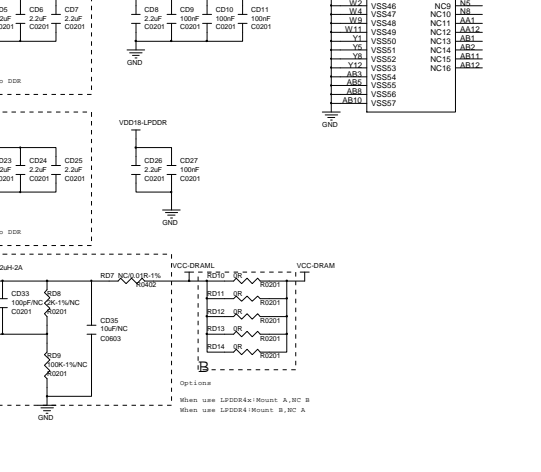
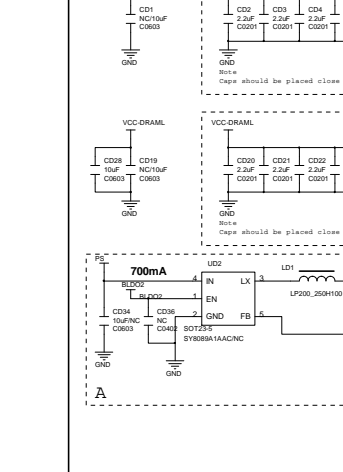
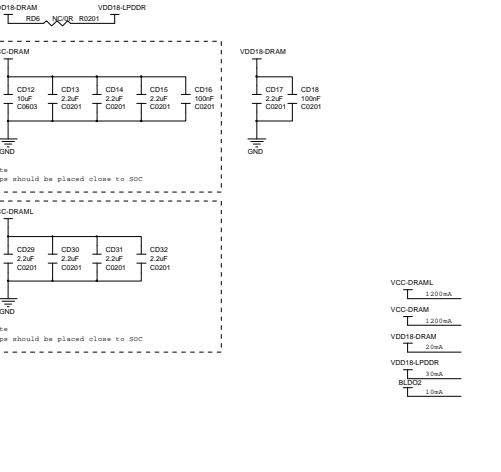
Allwinner Technology Co.,Ltd		
Design Name: A523-STD-AXP171C-AXP323-LPDDR4-4X		
Rev:	Page Name:	Rev:
E	07 POWER-AXP171C+AXP323	7
Date:	Wednesday, December 13, 2012 Sheet 7 of 23	

LPDDR4-4X

U1-A			LPDDR4-4X LPDDR4-4X				ZRank				4Rank				
SA0	SA1	SA2	SA3	SA4	SA5	SA6	SA7	SA8	SA9	SA10	SA11	SA12	SA13	SA14	SA15
AE29	AE28	AE27	AE26	AE25	AE24	AE23	AE22	AE21	AE20	AE19	AE18	AE17	AE16	AE15	AE14
AE13	AE12	AE11	AE10	AE09	AE08	AE07	AE06	AE05	AE04	AE03	AE02	AE01	AE00	AE00	AE00
AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00
AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00

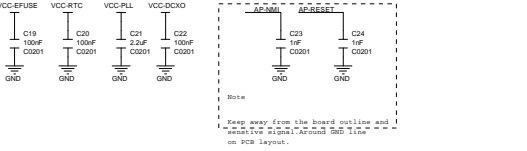
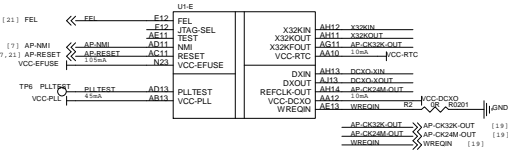
U1-B			LPDDR4-4X LPDDR4-4X				ZRank				4Rank				
SD04	SD03	SD02	SD01	SD00	SD00	SD01	SD02	SD03	SD04	SD04	SD03	SD02	SD01	SD00	SD00
AE29	AE28	AE27	AE26	AE25	AE24	AE23	AE22	AE21	AE20	AE19	AE18	AE17	AE16	AE15	AE14
AE13	AE12	AE11	AE10	AE09	AE08	AE07	AE06	AE05	AE04	AE03	AE02	AE01	AE00	AE00	AE00
AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00
AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00

U1-C			LPDDR4-4X LPDDR4-4X				ZRank				4Rank				
SD04	SD03	SD02	SD01	SD00	SD00	SD01	SD02	SD03	SD04	SD04	SD03	SD02	SD01	SD00	SD00
AE29	AE28	AE27	AE26	AE25	AE24	AE23	AE22	AE21	AE20	AE19	AE18	AE17	AE16	AE15	AE14
AE13	AE12	AE11	AE10	AE09	AE08	AE07	AE06	AE05	AE04	AE03	AE02	AE01	AE00	AE00	AE00
AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00
AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00	AE00

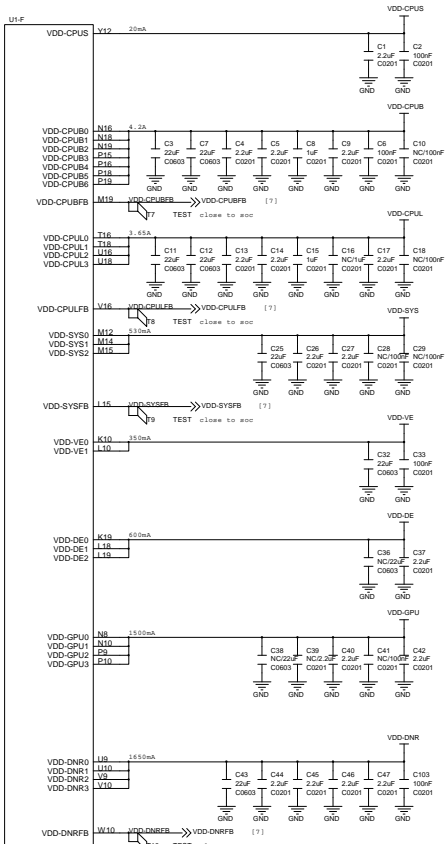


Options:
 A When use LPDDR4 Mount A, NC A
 B When use LPDDR4 Mount B, NC B

SYS

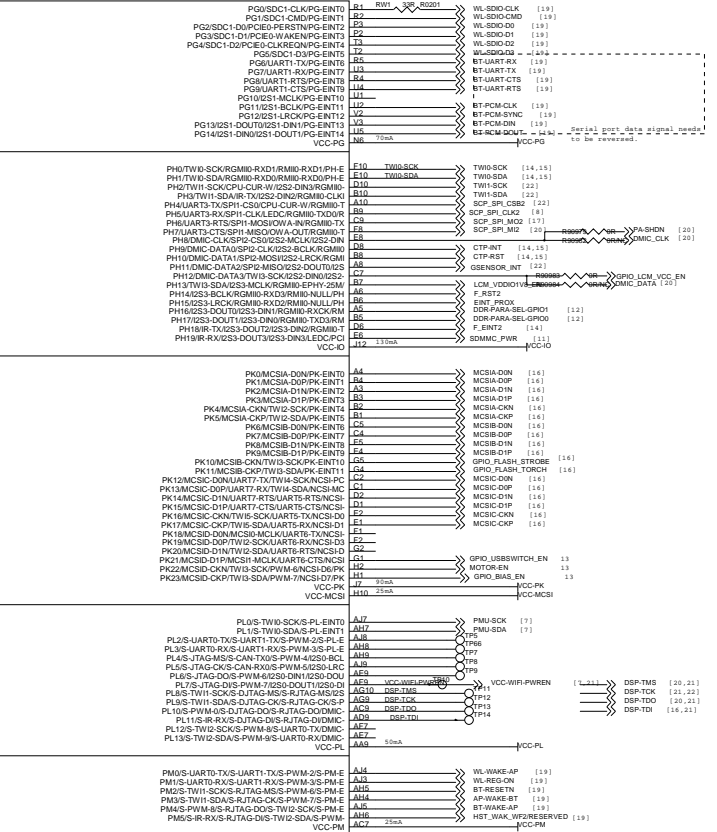
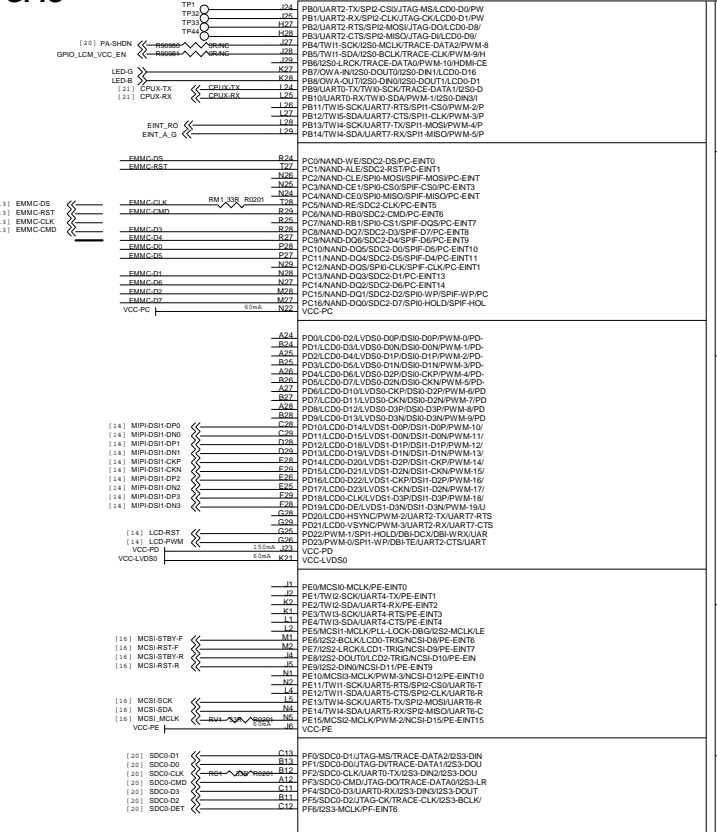


CORE POWER



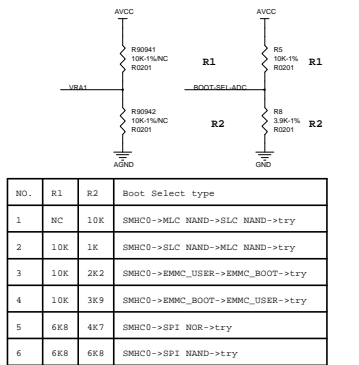
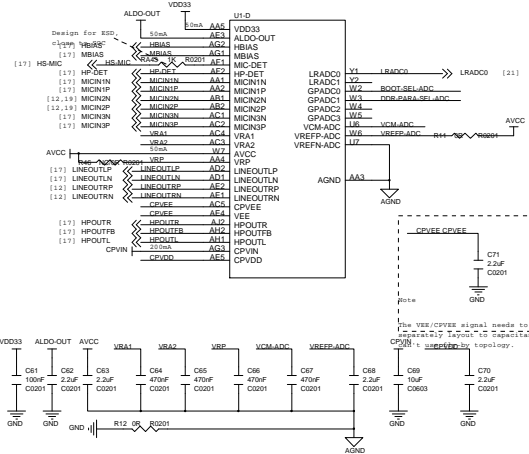
U1-G	GA1	GA2	GA3	GA4	GA5	GA6	GA7	GA8	GA9	GA10	GA11	GA12	GA13	GA14	GA15	GA16	GA17	GA18	GA19	GA20	GA21	GA22	GA23	GA24	GA25	GA26	GA27	GA28	GA29	GA30	GA31	GA32	GA33	GA34	GA35	GA36	GA37	GA38	GA39	GA40	GA41	GA42	GA43	GA44	GA45	GA46	GA47	GA48	GA49	GA50	GA51	GA52	GA53	GA54	GA55	GA56	GA57	GA58	GA59	GA60	GA61	GA62	GA63	GA64	GA65	GA66	GA67	GA68	GA69	GA70	GA71	GA72	GA73	GA74	GA75	GA76	GA77	GA78	GA79	GA80	GA81	GA82	GA83	GA84	GA85	GA86	GA87	GA88	GA89	GA90	GA91	GA92	GA93	GA94	GA95	GA96	GA97	GA98	GA99	GA100
------	-----	-----	-----	-----	-----	-----	-----	-----	-----	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	-------

GPIO



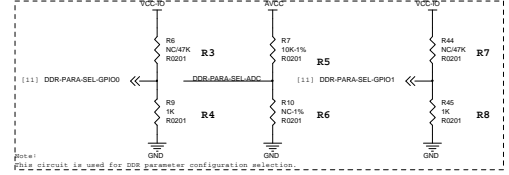
GPIO use side
 1. Note that the voltage of GND GND0 must match the external 2.0 voltage.
 2. The pull up voltage of the GPIO is selected to correspond to the power field voltage of GDD0.
 3. Power current in PCB layout reference mini1B2P

Audio&ADC



NO.	R1	R2	Boot Select type
1	NC	10K	SMHC0->MLC NAND->SLC NAND->try
2	10K	1K	SMHC0->SLC NAND->try
3	10K	2K2	SMHC0->EMMC_USER->EMMC_BOOT->try
4	10K	3K9	SMHC0->EMMC_BOOT->EMMC_USER->try
5	6K8	4K7	SMHC0->SPI NOR->try
6	6K8	6X8	SMHC0->SPI NAND->try

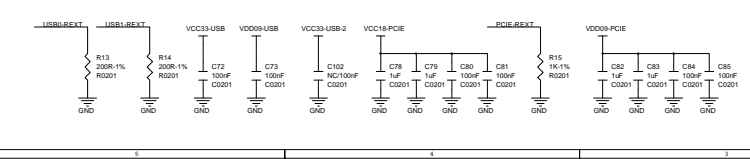
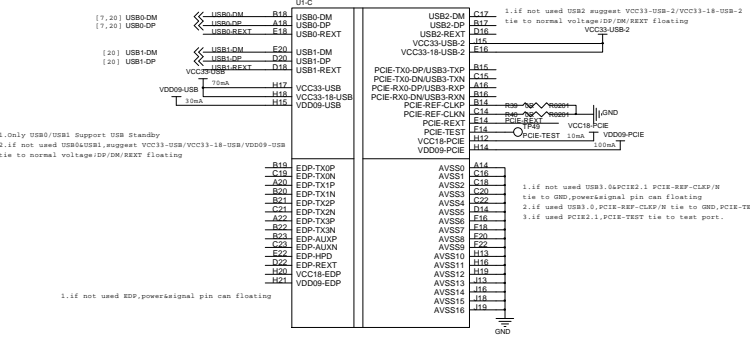
try default order:(selected fail media will not try)
EMMC_USER->EMMC_BOOT->SLC NAND->MLC NAND->SPI NOR->SPI NAND



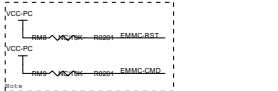
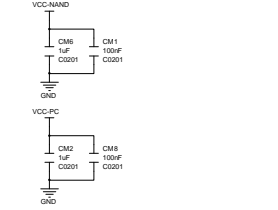
File: circuit is used for DDR parameter configuration selection

SPD0 enabled by the R1 pull-up and R2 pull-down resistance	SPD1 enabled by the R1 pull-up and R2 pull-down resistance	GRADC Voltage(Fixed pull-up R3 is 10K-1K, the voltage by adjusting pull-down resistance)	DDR PARA
0	0	382mV(2.7K-1K)	DDR PARA 0
0	0	608mV(5.1K-1K)	DDR PARA 1
0	0	811mV(8.2K-1K)	DDR PARA 2
0	0	1050mV(14K-1K)	DDR PARA 3
0	0	1315mV(27K-1K)	DDR PARA 4
0	0	1569mV(68K-1K)	DDR PARA 5
0	0	1800mV(NC)	DDR PARA 6
0	1	163mV(1K-1K)	DDR PARA 7
0	1	382mV(2.7K-1K)	DDR PARA 8
0	1	608mV(5.1K-1K)	DDR PARA 9
0	1	811mV(8.2K-1K)	DDR PARA 10
0	1	1050mV(14K-1K)	DDR PARA 11
0	1	1315mV(27K-1K)	DDR PARA 12
0	1	1569mV(68K-1K)	DDR PARA 13
0	1	1800mV(NC)	DDR PARA 14
1	0	163mV(1K-1K)	DDR PARA 15
1	0	382mV(2.7K-1K)	DDR PARA 16
1	0	608mV(5.1K-1K)	DDR PARA 17
1	0	811mV(8.2K-1K)	DDR PARA 18
1	0	1050mV(14K-1K)	DDR PARA 19
1	0	1315mV(27K-1K)	DDR PARA 20
1	0	1569mV(68K-1K)	DDR PARA 21
1	0	1800mV(NC)	DDR PARA 22
1	1	163mV(1K-1K)	DDR PARA 23
1	1	382mV(2.7K-1K)	DDR PARA 24
1	1	608mV(5.1K-1K)	DDR PARA 25
1	1	811mV(8.2K-1K)	DDR PARA 26
1	1	1050mV(14K-1K)	DDR PARA 27
1	1	1315mV(27K-1K)	DDR PARA 28
1	1	1569mV(68K-1K)	DDR PARA 29
1	1	1800mV(NC)	DDR PARA 30
1	1	1800mV(NC)	DDR PARA 31

USB&EDP&PCIE

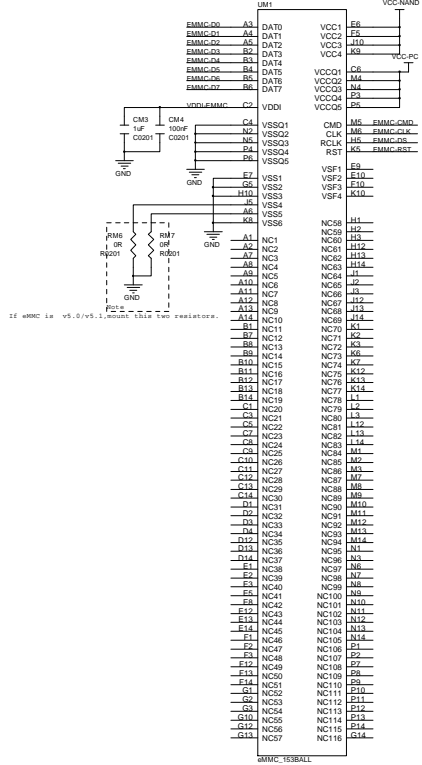


EMMC Default:use EMMC

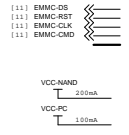
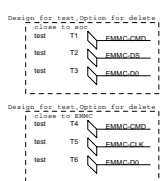


EMMC-RST and EMMC-CMD signals are internally pulled up in the SOC. RM10 and RM11 can omit down.
 EMMC-CLK and EMMC-DS signals are internally pulled down in the SOC. RM12 and RM13 can omit down.

If use EMMC is not v5.0/v5.1, then RC this resistor. EMMC-DS signals are internally pulled down in the SOC. RM10 can omit down.

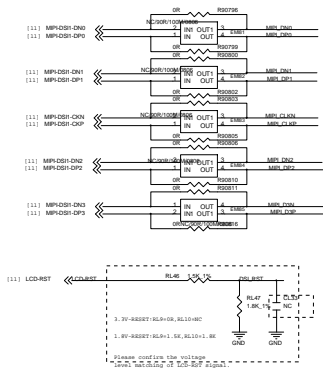


EMMC_153BALL

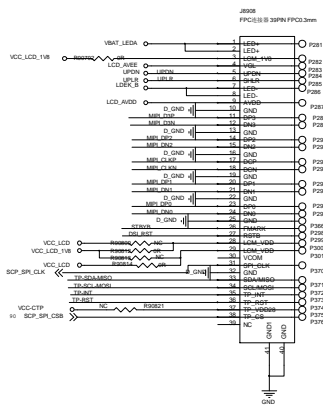


- [11] EMMC-DS
- [11] EMMC-RST
- [11] EMMC-CLK
- [11] EMMC-CMD

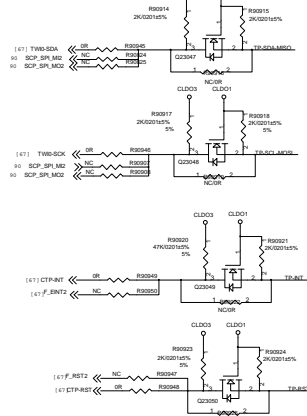
LCM Power



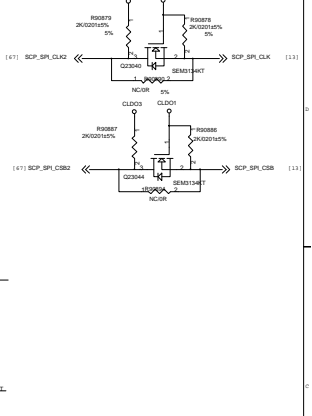
Main LCM



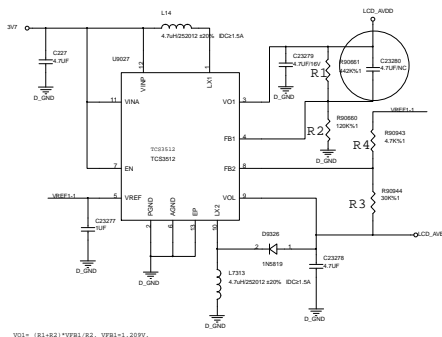
I2C



SPI

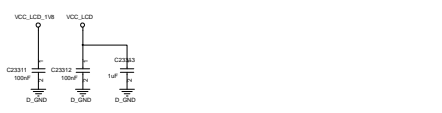


偏压

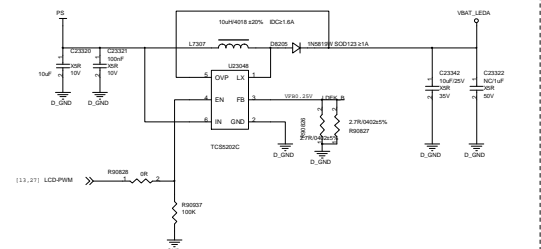


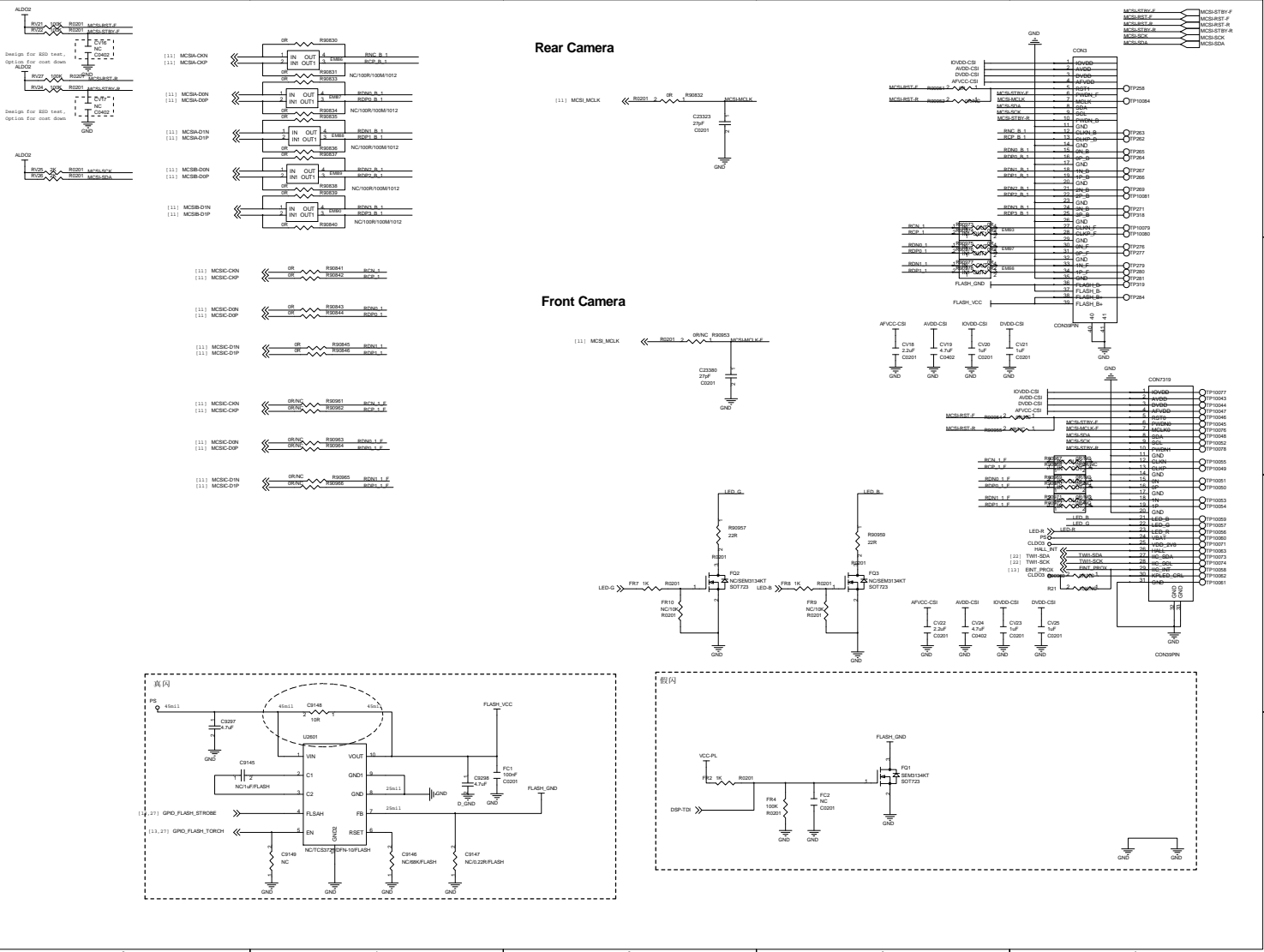
$$V_{O1} = (R1+R2) \cdot V_{FB1}/R2, V_{FB1} = 1.209V$$

$$V_{O2} = V_{FB2} - (V_{FB2} - V_{FB1}) \cdot R3/R4, V_{FB2} = 0.257V, V_{FB1} = 1.209V$$



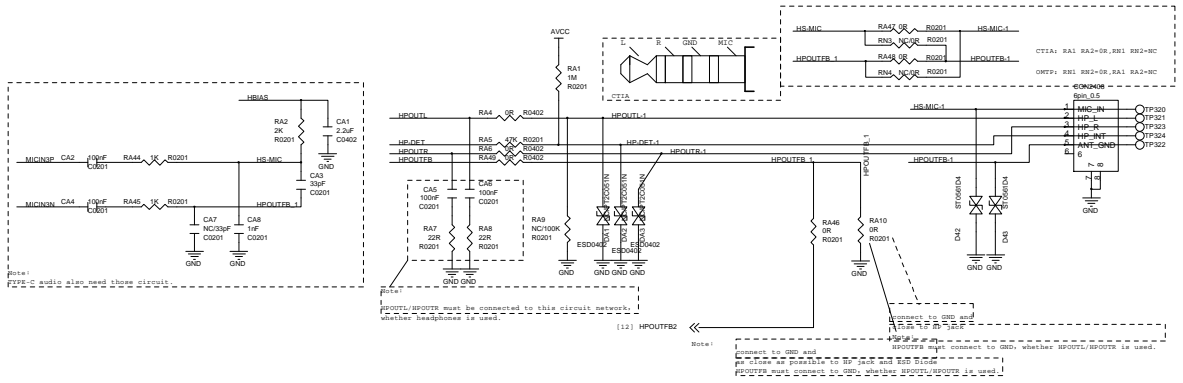
背光



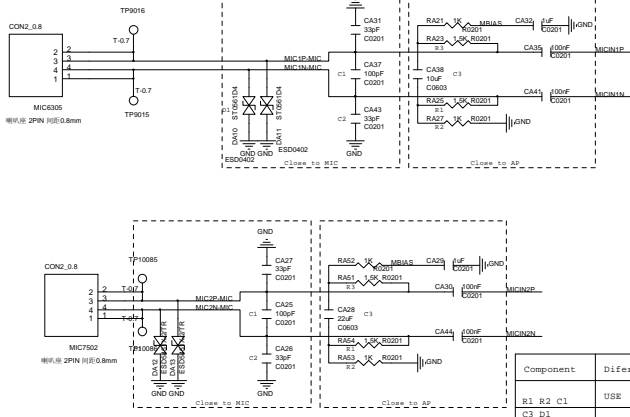


HEADPHONE

- [12] MICIN1P <<< MICIN1P
- [12] MICIN1N <<< MICIN1N
- [12] HS-MIC <<< HS-MIC
- [12] HBAS <<< HBAS
- [12] HP-OUTL <<< HP-OUTL
- [12] HP-OUTR <<< HP-OUTR
- [12] HP-DET <<< HP-DET
- [12] MBAS <<< MBAS
- [12] MICIN1P <<< MICIN1P
- [12] MICIN1N <<< MICIN1N
- [12,19] MICIN2P <<< MICIN2P
- [12,19] MICIN2N <<< MICIN2N

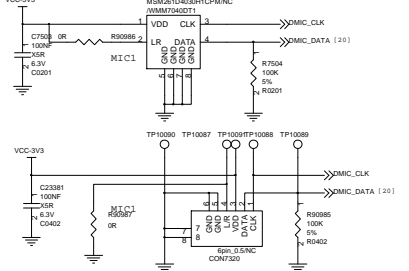


ECM MIC



Component	Diferential	single-ended
R1 R2 C1	USE	NC
C3 D1	33pF	DR
R3	2.2K	1K

DMIC MAIN

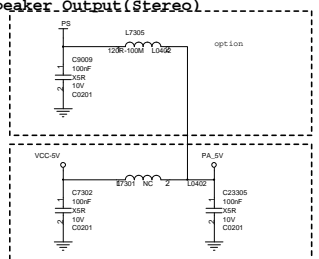


>>>HPOUTL 19,30
 >>>HPOUTR 19,30
 >>>PA_SHDN 12

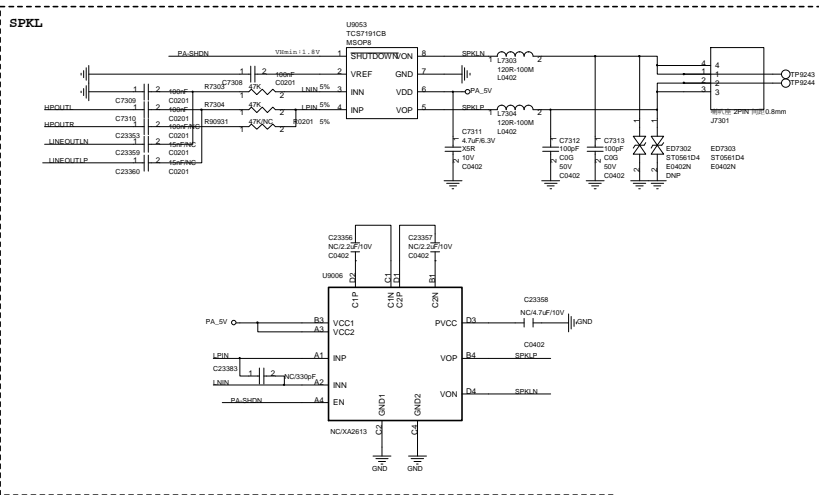
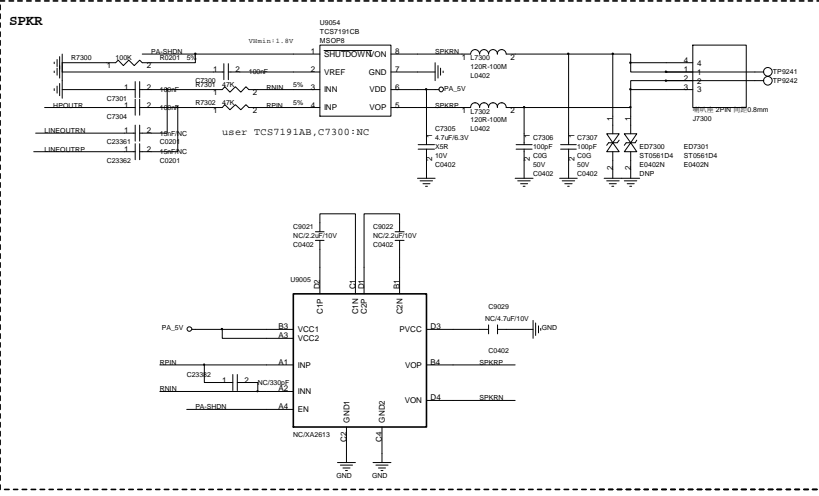
[12] LINEOUTHP <<<LINEOUTSR
 [12] LINEOUTHN <<<LINEOUTSH
 [12] LINEOUTLP <<<LINEOUTSL
 [12] LINEOUTLN <<<LINEOUTSLN

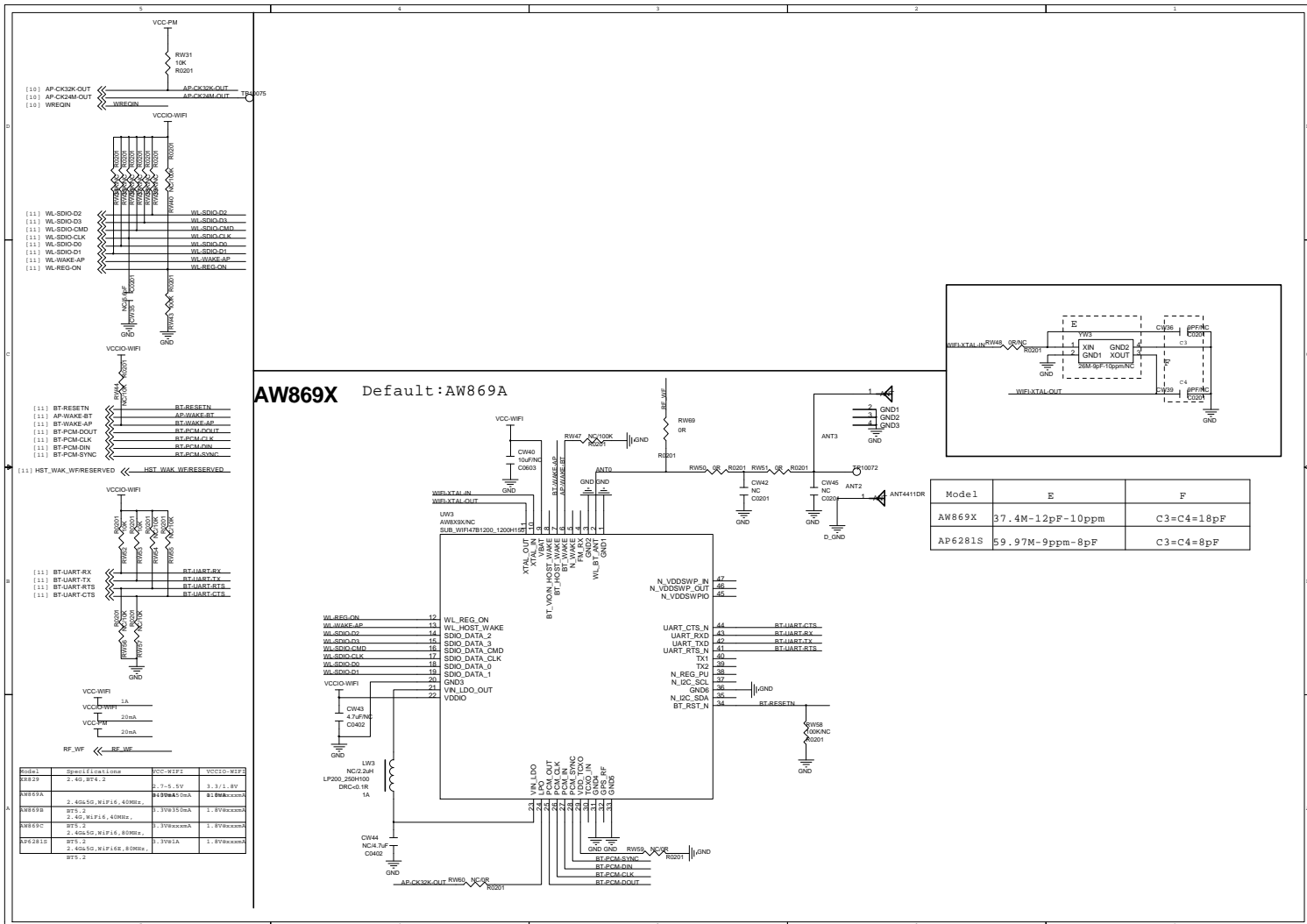
Application Option: 2x Speaker Output

Speaker_Output (Stereo)



Maximum power supply capacity from RK817-5
 MINO path is 1.5A.
 For high-power amplifier design, an external
 boost circuit is needed, and the boost circuit
 can directly take power from the VBAT.



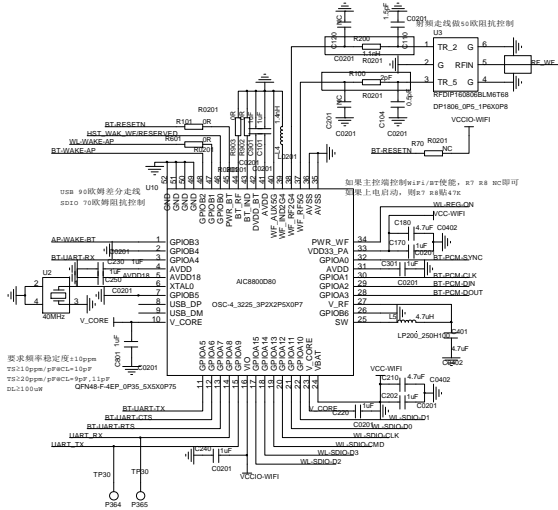
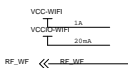


- [11] WL_SDIO_D2 << WL_SDIO_D2
- [11] WL_SDIO_D3 << WL_SDIO_D3
- [11] WL_SDIO_CMD << WL_SDIO_CMD
- [11] WL_SDIO_CLK << WL_SDIO_CLK
- [11] WL_SDIO_D0 << WL_SDIO_D0
- [11] WL_SDIO_D1 << WL_SDIO_D1
- [11] WL_WAKE_AP << WL_WAKE_AP
- [11] WL_REG_ON << WL_REG_ON

HST_WAK_WFRRESERVED << R9028 NCOR >> HST_WAK_WFRRESERVED

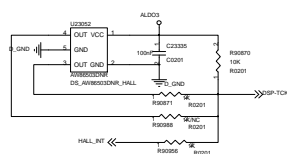
- [11] BT_RESETN << BT_RESETN
- [11] AP_WAKE_BT << AP_WAKE_BT
- [11] BT_WAKE_AP << BT_WAKE_AP
- [11] BT_PCM_OUT << BT_PCM_OUT
- [11] BT_PCM_CLK << BT_PCM_CLK
- [11] BT_PCM_DIN << BT_PCM_DIN
- [11] BT_PCM_SYNC << BT_PCM_SYNC

- [11] BT_UART_RX << BT_UART_RX
- [11] BT_UART_TX << BT_UART_TX
- [11] BT_UART_RTS << BT_UART_RTS
- [11] BT_UART_CTS << BT_UART_CTS

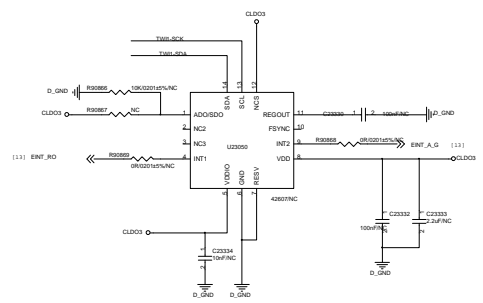




霍尔开关

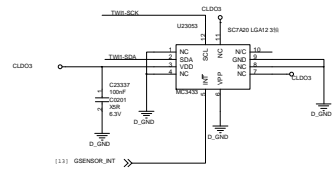


Gyro Sensor

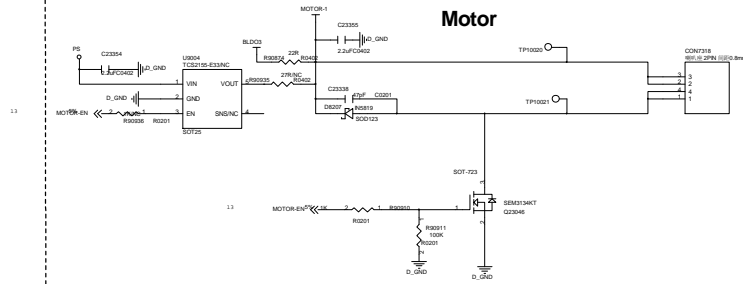


ALS&PROX

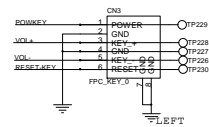
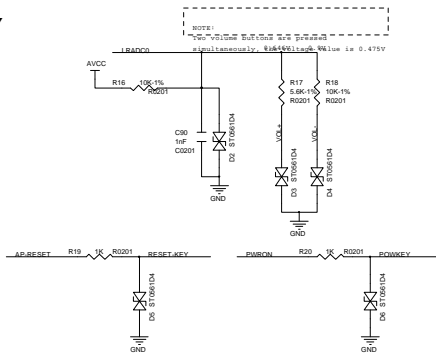
Gsensor



Motor



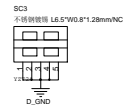
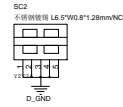
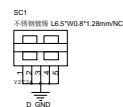
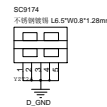
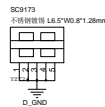
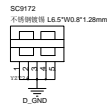
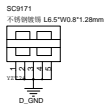
KEY



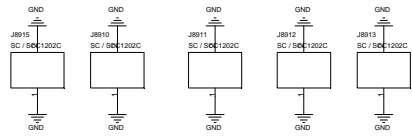
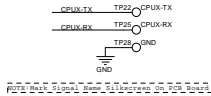
- [7, 10] AP-RESET <<< AP-RESET
- [12] LRADCC <<< LRADCC
- [7] PWRON <<< PWRON
- [10] FEL <<< FEL

- [11] CPUX-TX <<< CPUX-TX
- [11] CPUX-RX <<< CPUX-RX

SHIELD



CPUX DEBUG



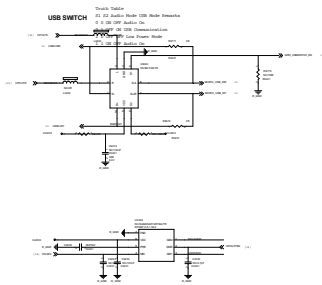
MARK POINT



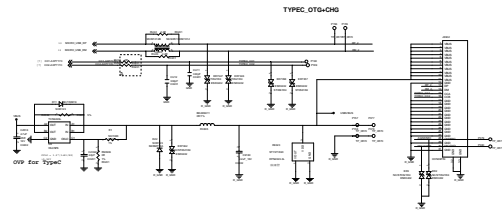
FEL



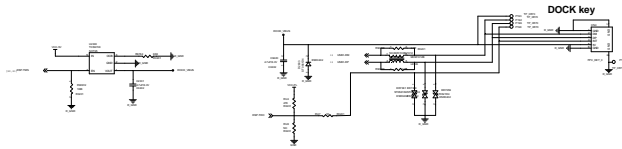
TYPE-C 耳机



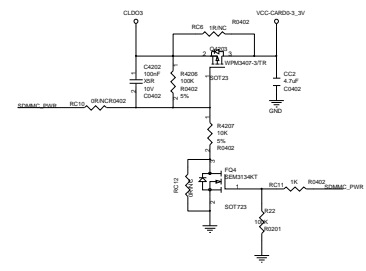
TYPE-C USB



DOCKING OTG



- [11] SDIO-D1
- [11] SDIO-D0
- [11] SDIO-CLK
- [11] SDIO-CD
- [11] SDIO-DE
- [11] SDMMC_PWR



SD CARD

