

VERSION HISTORY

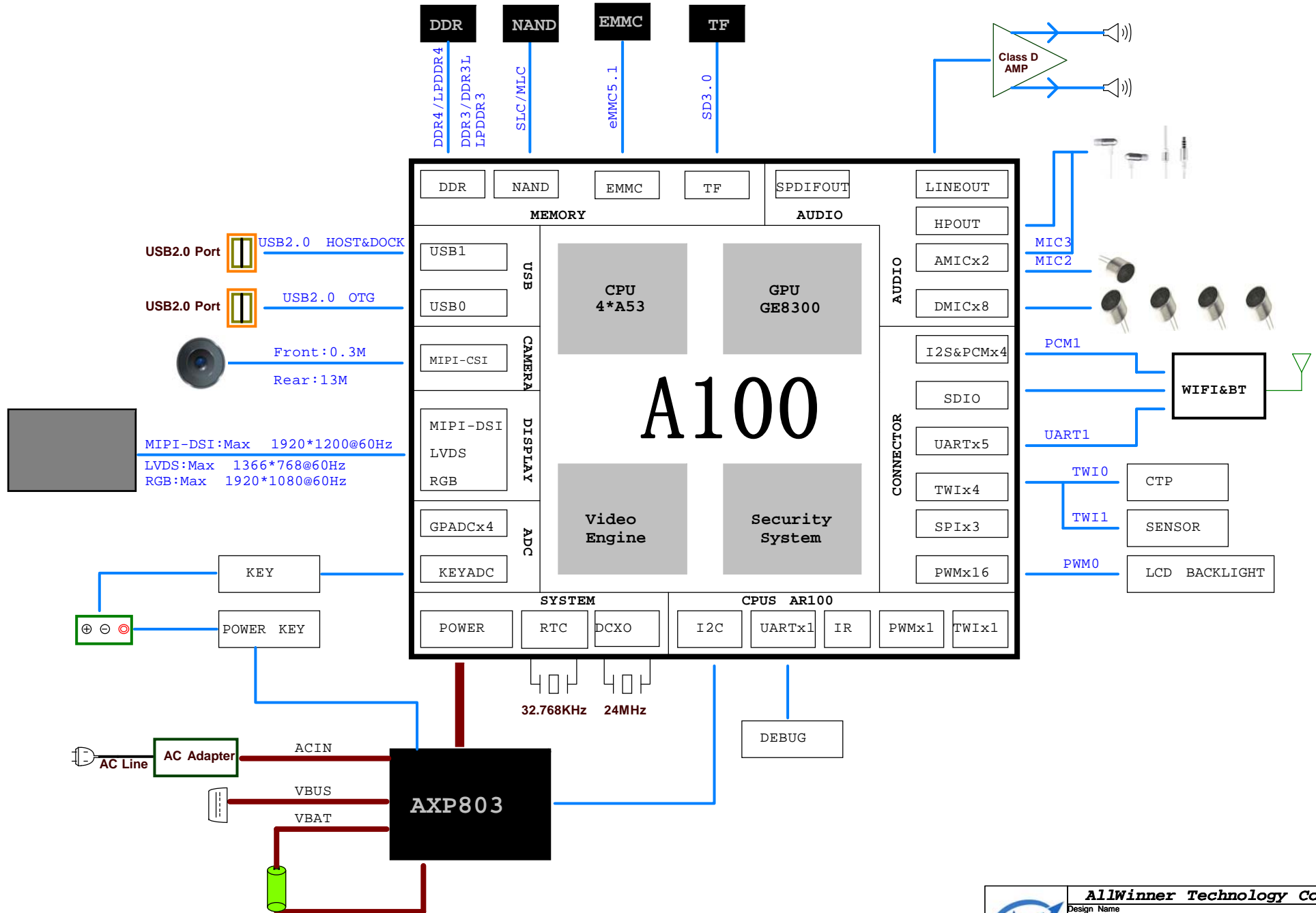
M110F6 Circuit diagram

Index:

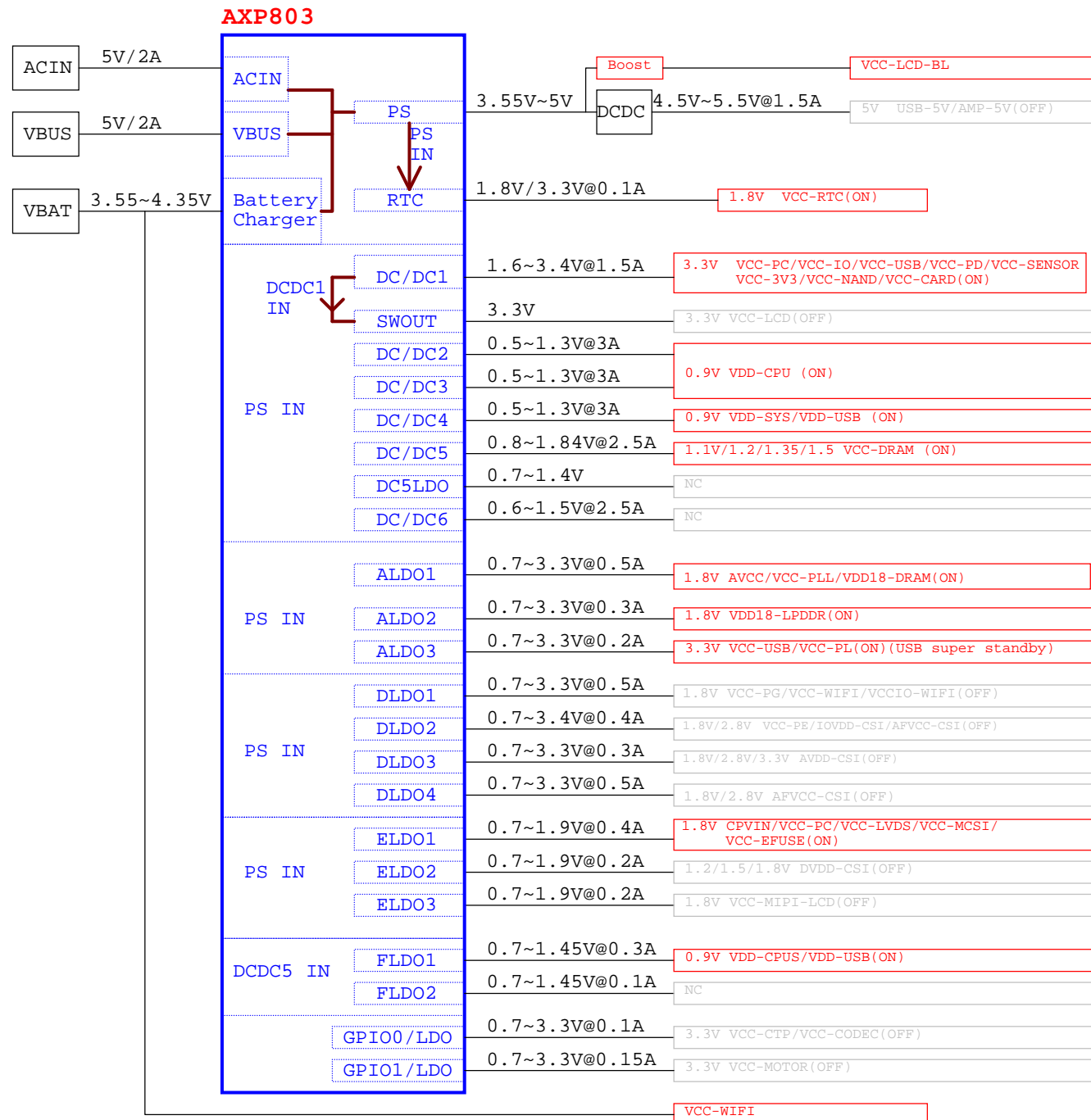
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- P12 CAMREA
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- P16 WIFI+BT
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- P17 AC101

Revision	Description	Date	Drawn	Checked	Approved
Ver 1.0	Releas version	2019-12-20	LQS		

BLOCK



DEFAULT POWER ON
 DEFAULT POWER OFF



GPIO ASSIGNMENT

PIN	Define	CFG	Function
PB0	CPUX_TMS	4	DEBUG
PB1	CPUX_TCK	4	
PB2	CPUX_TDO	4	
PB3	CPUX_TDI/IRQ-AUDIO	4	
PB4	I2S0-MCLK		GPIO
PB5	I2S0-BCLK		
PB6	I2S0-LRCK		
PB7	I2S0-DOUT		
PB8	LCD-BL-EN	3	DEBUG
PB9	CPUX_TX	2	
PB10	CPUX_RX	2	

PIN	Define	CFG	Function
PE0	MCSI_MCLK	2	CSI
PE1	MCSI_SCK	2	
PE2	MCSI_SDA	2	
PE3			
PE4			
PE5			
PE6	MCSIB_STBY_F	1	
PE7	MCSIB_RST_F	1	
PE8	MCSIA_STBY_R	1	
PE9	MCSIA_RST_R	1	

PIN	Define	CFG	Function
PH0	TWI0_SCK	2	TWI
PH1	TWI0_SDA	2	
PH2	TWI1_SCK	2	
PH3	TWI1_SDA	2	GPIO
PH4	PS-EINT	1	
PH5			
PH6	PA_SHDN	0	
PH7			
PH8	USB0_ID_SOC	0	
PH9	CTP_INT	0	
PH10	CTP_RST	1	
PH11	GS-INT	0	
PH12			
PH13			
PH14			
PH15			
PH16			
PH17			
PH18			
PH19			

PIN	Define	CFG	Function
PC0	NAND_WE/SDC2_DS	2/3	NAND/eMMC
PC1	NAND_ALE/SDC2_RST	2/3	
PC2	NAND_CLE	2	
PC3	NAND_CE1	2	
PC4	NAND_CE0	2	
PC5	NAND_RE/SDC2_CLK	2/3	
PC6	NAND_RB0/SDC2_CMD	2/3	
PC7	NAND_RB1	2	
PC8	NAND_DQ7/SDC2_D3	2/3	
PC9	NAND_DQ6/SDC2_D4	2/3	
PC10	NAND_DQ5/SDC2_D0	2/3	
PC11	NAND_DQ4/SDC2_D5	2/3	
PC12	NAND_DQS	2	
PC13	NAND_DQ3/SDC2_D1	2/3	
PC14	NAND_DQ2/SDC2_D6	2/3	
PC15	NAND_DQ1/SDC2_D2	2/3	
PC16	NAND_DQ0/SDC2_D7	2/3	

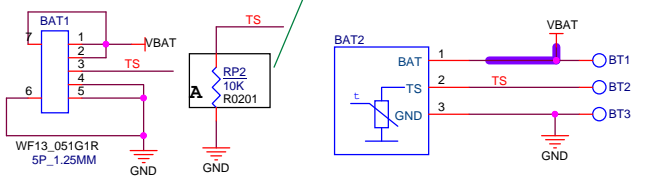
PIN	Define	CFG	Function
PF0	SDC0_D1	2	CARD
PF1	SDC0_D0	2	
PF2	SDC0_CLK	2	
PF3	SDC0_CMD	2	
PF4	SDC0_D3	2	
PF5	SDC0_D2	2	
PF6	SDC0_DET	0	

PIN	Define	CFG	Function
PL0	PMU_SCK	2	CPUS
PL1	PMU_SDA	2	
PL2	BT_RST_N	1	
PL3	BT_WAKE_AP	0	
PL4	AP_WAKE_BT	1	
PL5	WL_PMU_EN	1	
PL6	WL_WAKE_AP	0	
PL7	CPUS-TDI		
PL8	USB1-DRVVBUS		
PL9	EINT-HAL		
PL10	KD-EINT		
PL11	LED-EN	3	

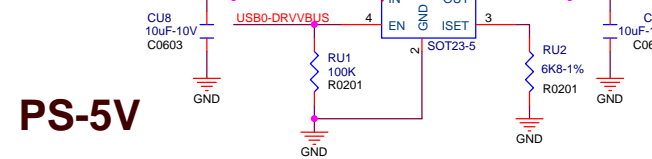
PIN	Define	CFG	Function
PD0	LCD_D2	2	LCD
PD1	LCD_D3	2	
PD2	LCD_D4	2	
PD3	LCD_D5	2	
PD4	LCD_D6	2	
PD5	LCD_D7	2	
PD6	LCD_D10	2	
PD7	LCD_D11	2	
PD8	LCD_D12	2	
PD9	LCD_D13	2	
PD10			
PD11			
PD12			
PD13			
PD14			
PD15			
PD16			
PD17			
PD18			
PD19			
PD20			
PD21			
PD22	LCD_RST	1	
PD23	LCD_PWM	3	

PIN	Define	CFG	Function
PG0	WL_SDIO_CLK	2	WIFI/BT
PG1	WL_SDIO_CMD	2	
PG2	WL_SDIO_D0	2	
PG3	WL_SDIO_D1	2	
PG4	WL_SDIO_D2	2	
PG5	WL_SDIO_D3	2	
PG6	BT_UART_RX	2	
PG7	BT_UART_TX	2	
PG8	BT_UART_CTS	2	
PG9	BT_UART_RTS	2	
PG10	BT_PCM_CLK	3	
PG11	BT_PCM_SYNC	3	
PG12	BT_PCM_DIN	3	
PG13	BT_PCM_DOUT	3	

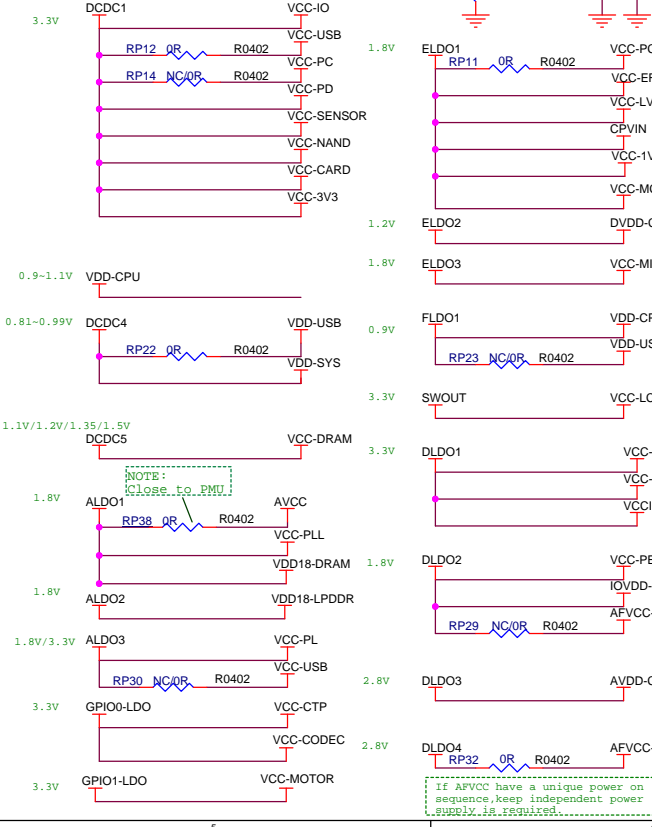
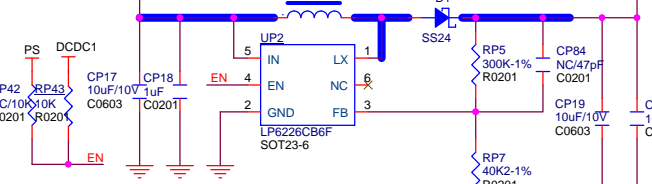
BAT



5V-VBUS

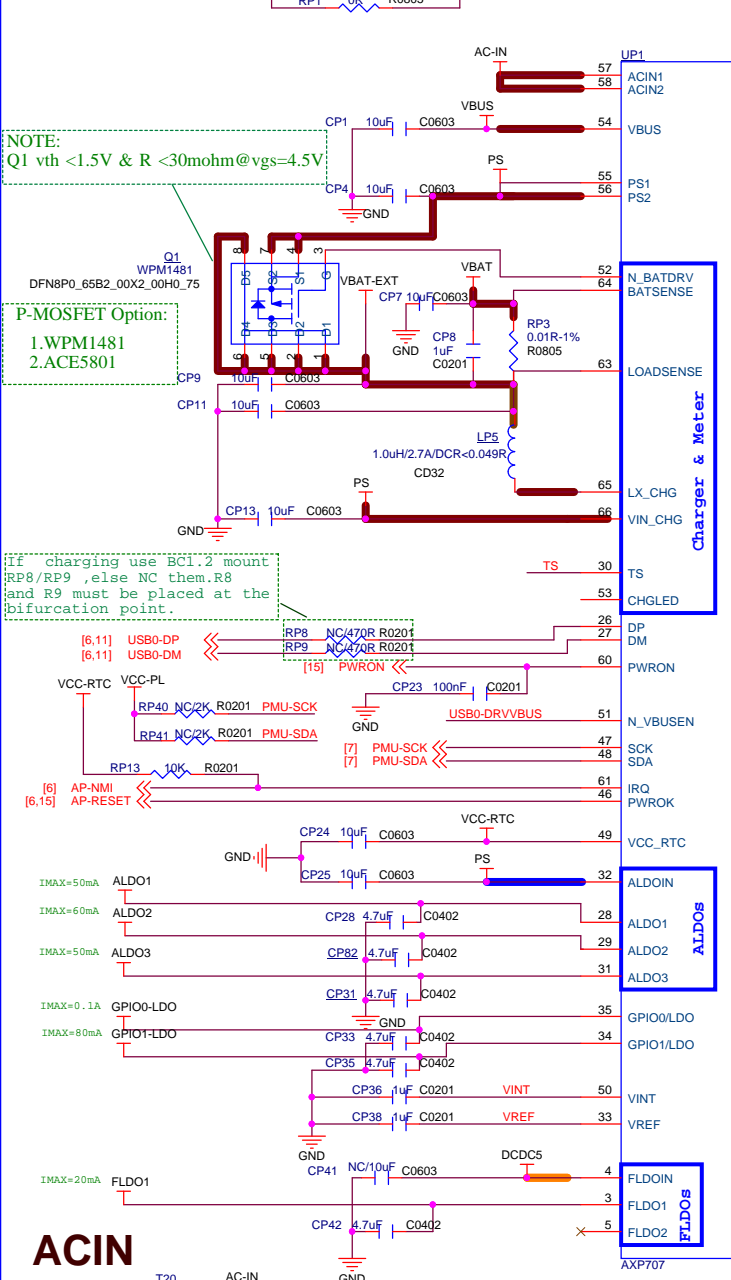


PS-5V

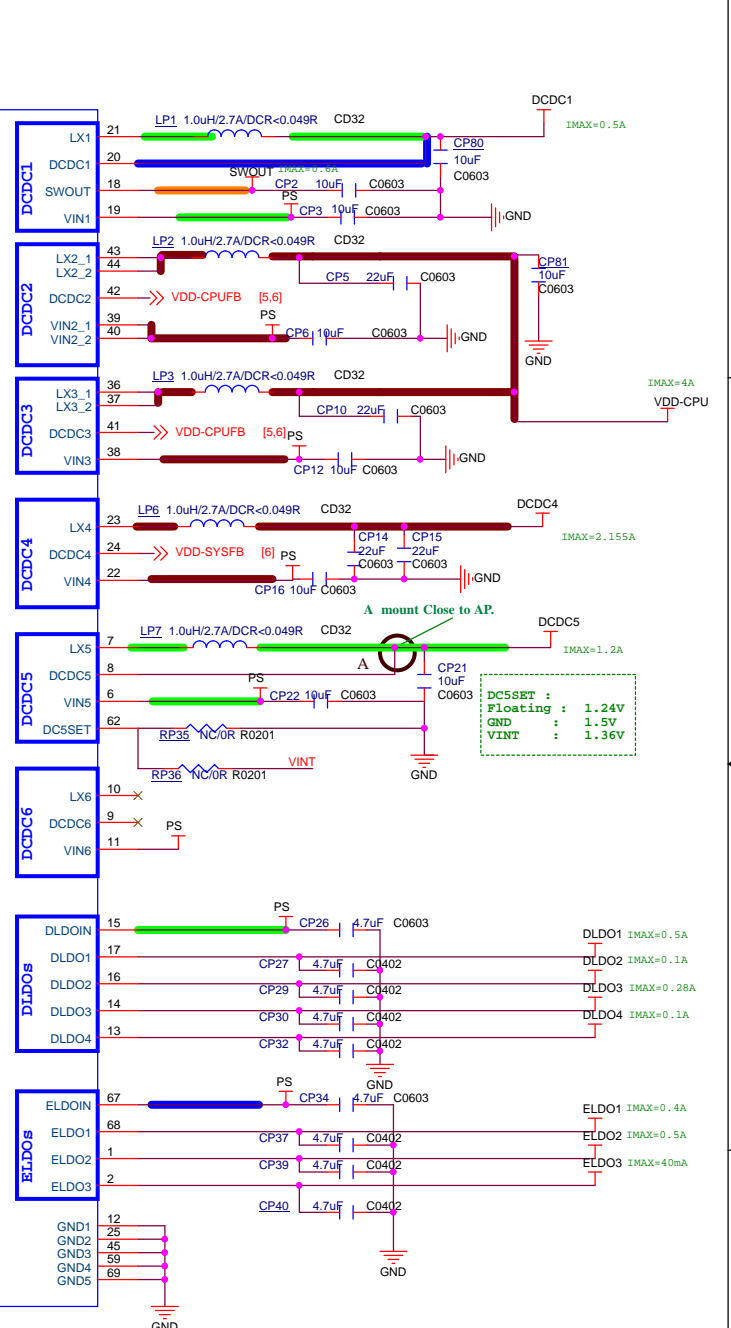
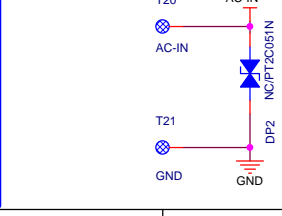


NOTE: If AVCC have a unique power on sequence, keep independent power supply is required.

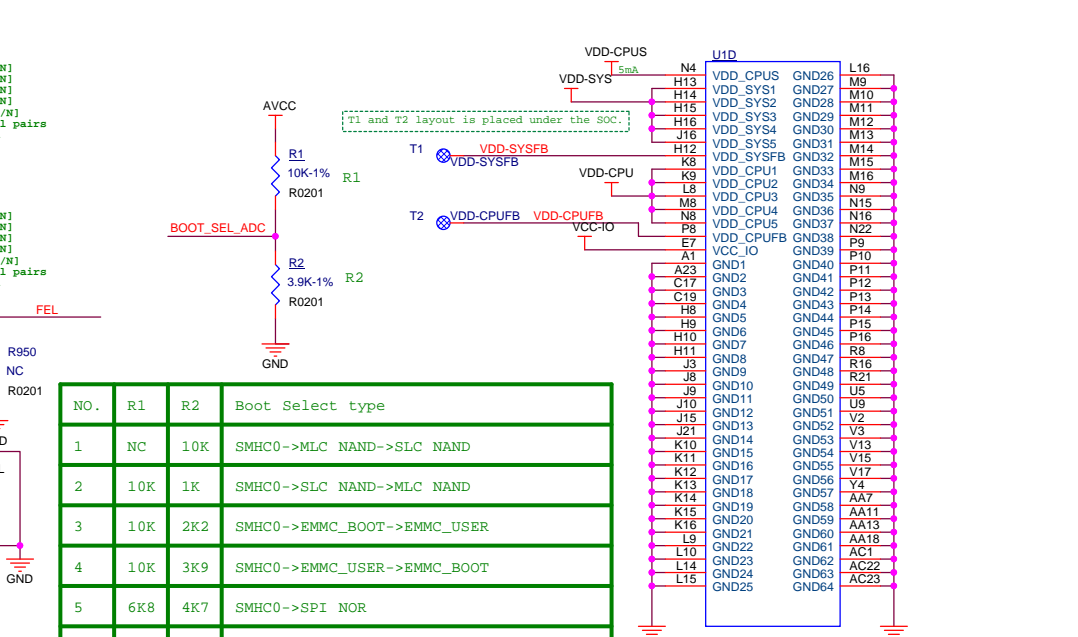
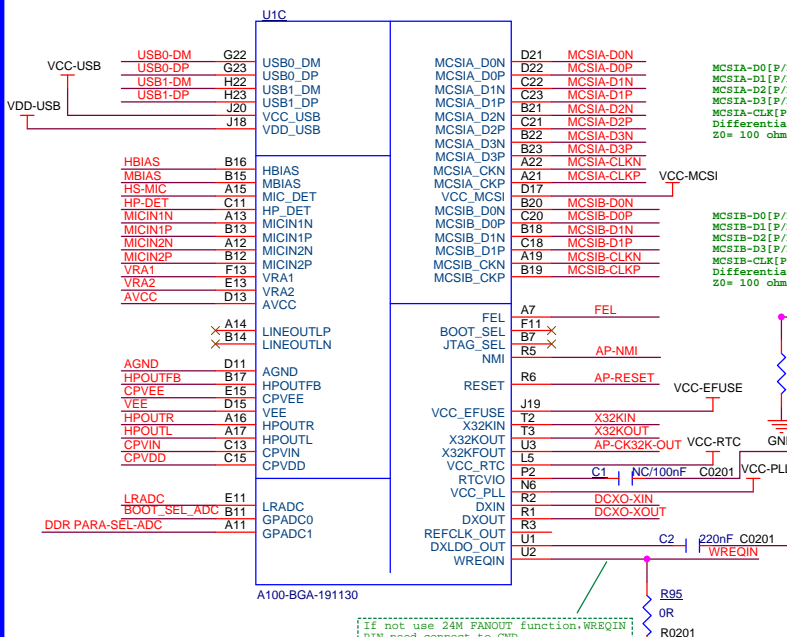
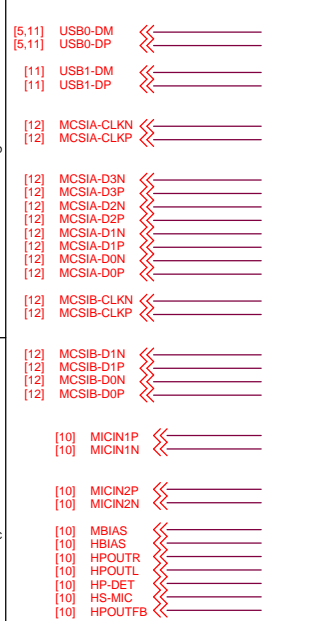
PMIC



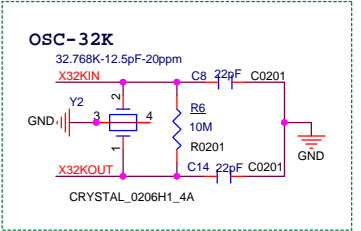
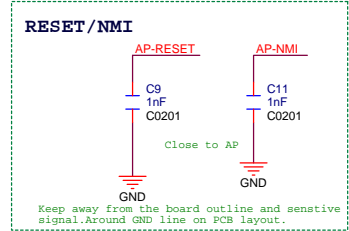
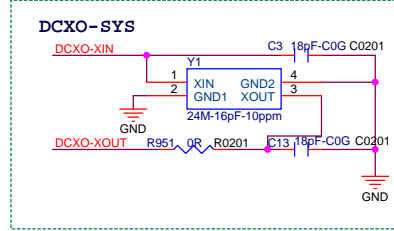
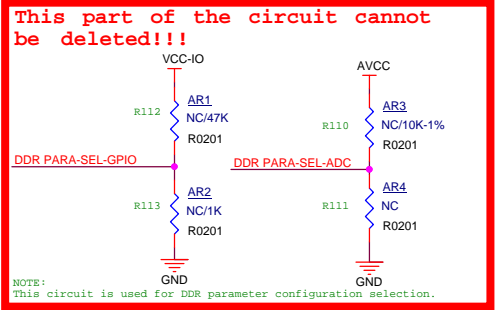
ACIN



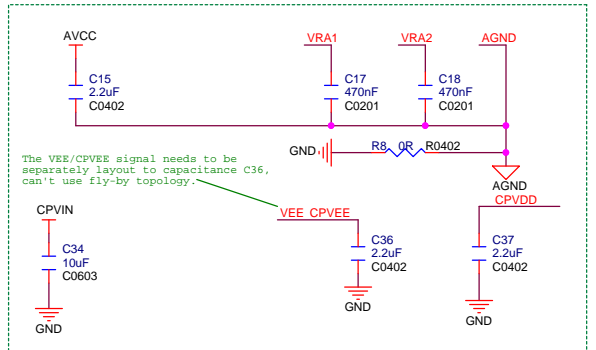
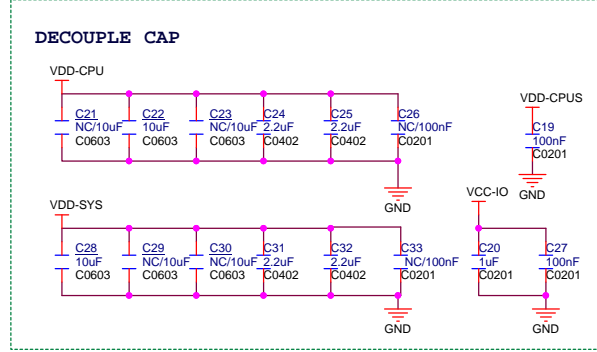
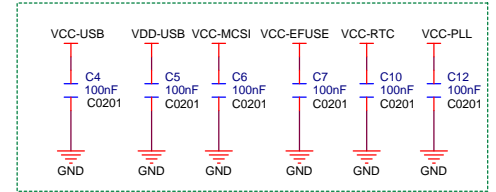
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		Design Name	A100_B3_AXP707_LPDDR3
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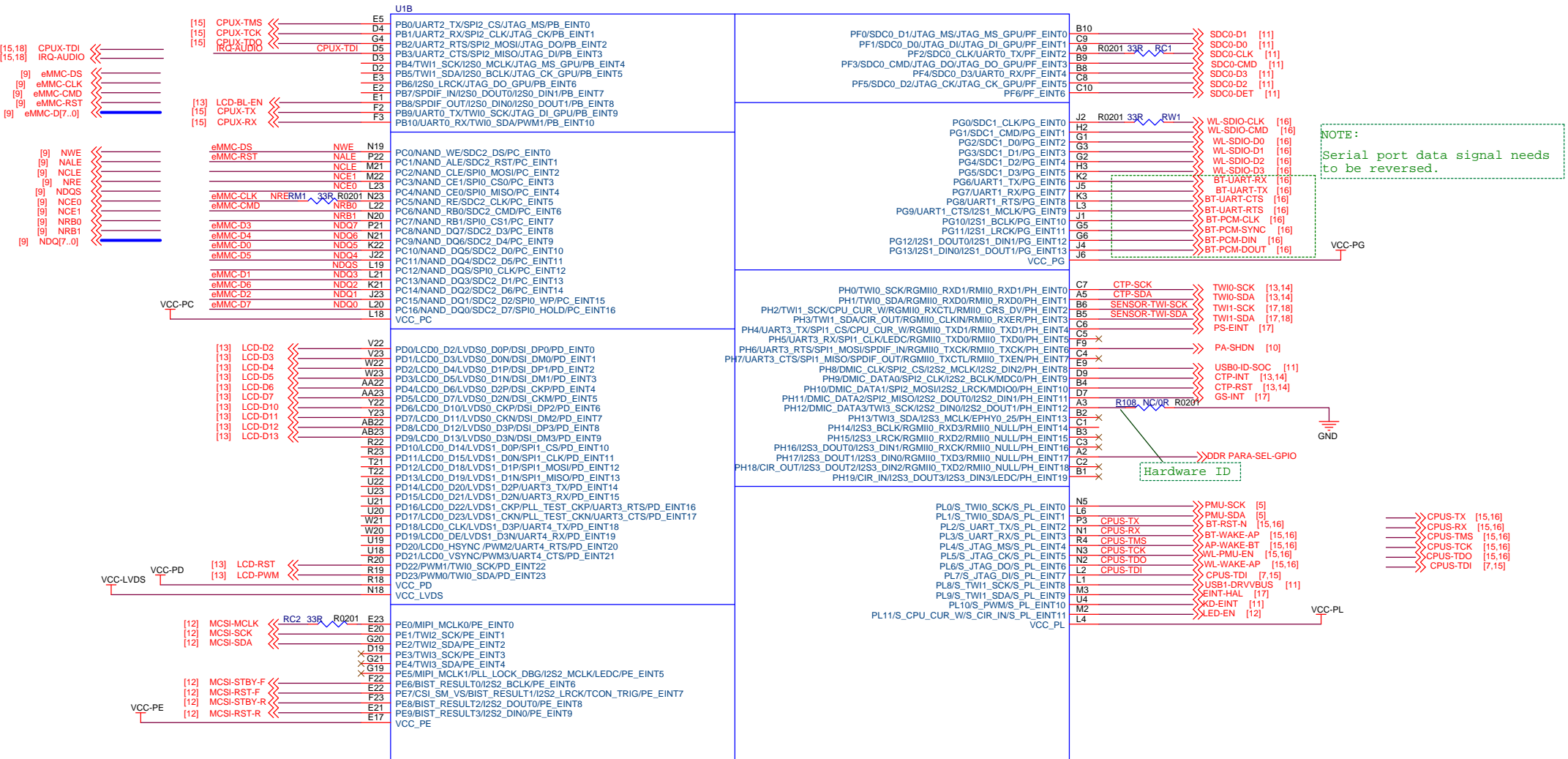
NO.	R1	R2	Boot Select type
1	NC	10K	SMHC0->MLC NAND->SLC NAND
2	10K	1K	SMHC0->SLC NAND->MLC NAND
3	10K	2K2	SMHC0->EMMC_BOOT->EMMC_USER
4	10K	3K9	SMHC0->EMMC_USER->EMMC_BOOT
5	6K8	4K7	SMHC0->SPI NOR
6	6K8	6K8	SMHC0->SPI NAND



GPIO Level(Set by the R112 pull-up and R113 pull-down resistance of PH17 GPIO)	GPADC Voltage(Fixed pull-up R110 i 10K-1K, Set the voltage by adjusting pull-down resistor R11)	DDR PARA
0	163mV(1K-1%)	DDR PARA 1
0	382mV(2.7K-1%)	DDR PARA 2
0	608mV(5.1K-1%)	DDR PARA 3
0	811mV(8.2K-1%)	DDR PARA 4
0	1050mV(14K-1%)	DDR PARA 5
0	1315mV(27K-1%)	DDR PARA 6
0	1569mV(68K-1%)	DDR PARA 7
0	1800mV(NC)	DDR PARA 8
1	163mV(1K-1%)	DDR PARA 9
1	382mV(2.7K-1%)	DDR PARA 10
1	608mV(5.1K-1%)	DDR PARA 11
1	811mV(8.2K-1%)	DDR PARA 12
1	1050mV(14K-1%)	DDR PARA 13
1	1315mV(27K-1%)	DDR PARA 14
1	1569mV(68K-1%)	DDR PARA 15
1	1800mV(NC)	DDR PARA 16

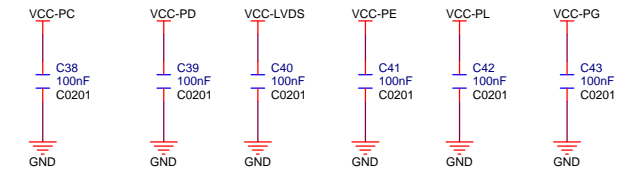


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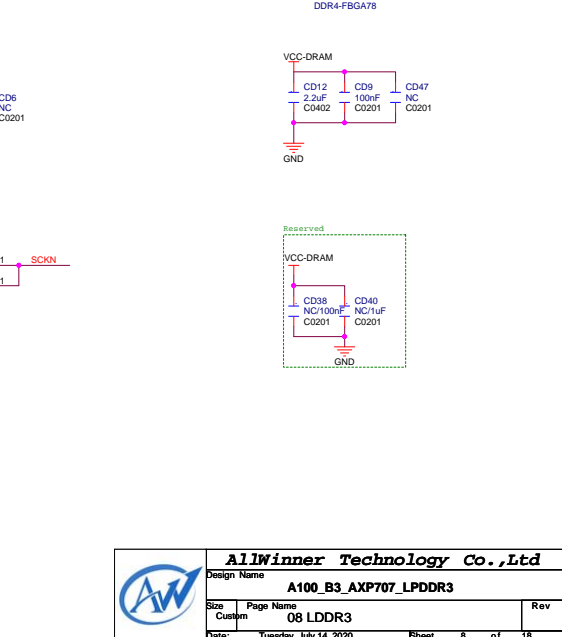
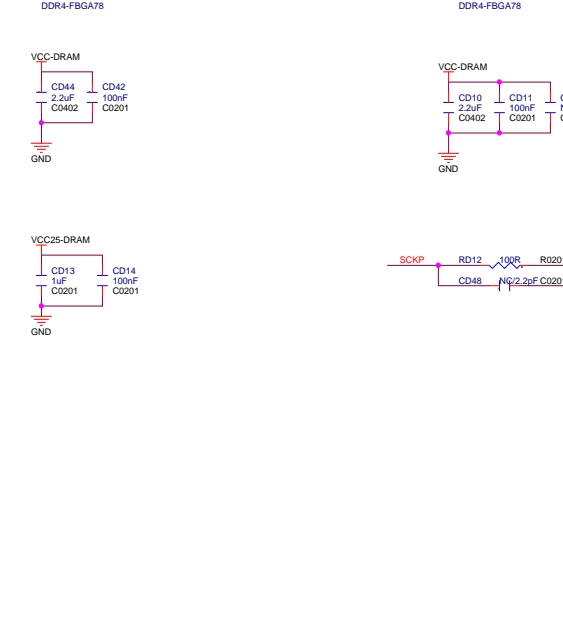
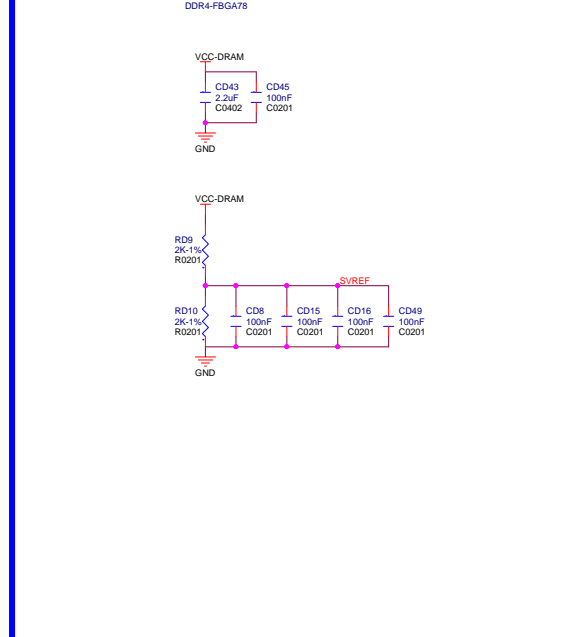
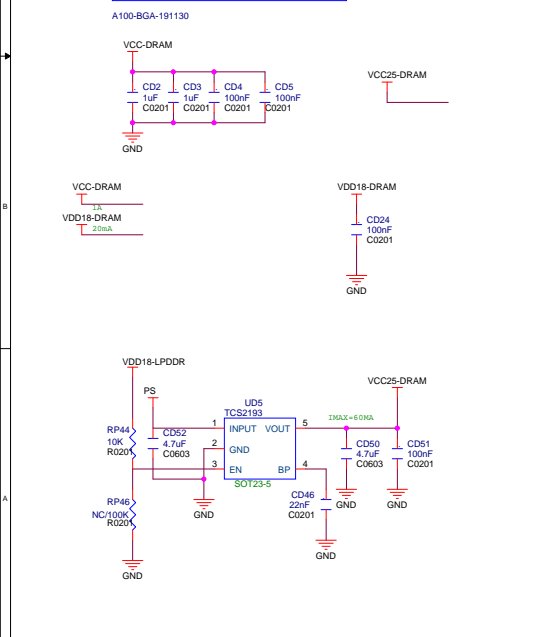
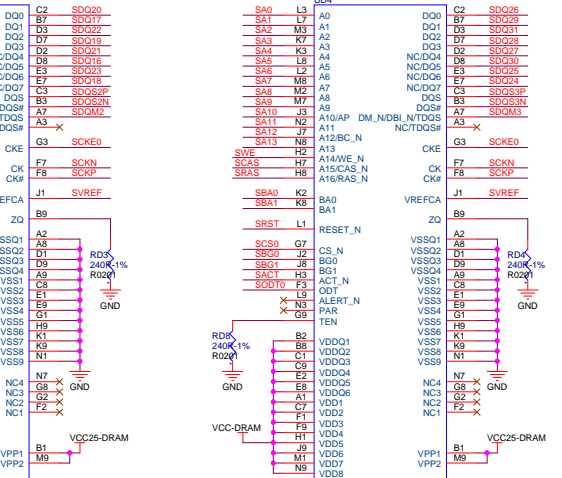
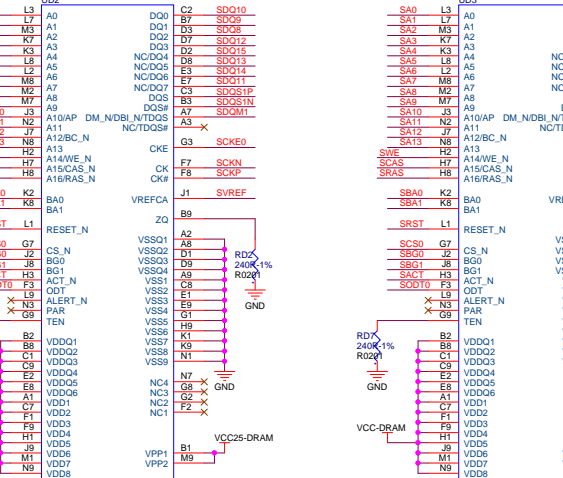
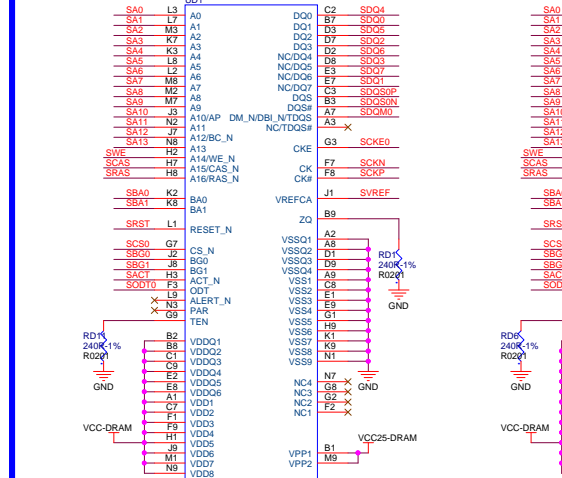
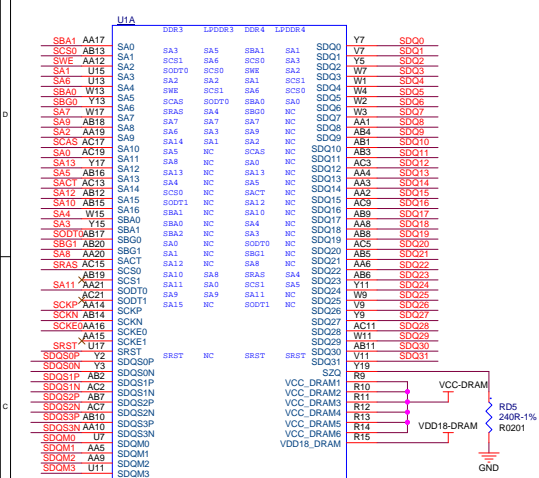


GPIO use guide:

1. Note that the voltage of SOC GPIO must matches the external IO voltage.
2. The pull up voltage of the GPIO is selected to correspond to the power field voltage of GPIO.



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AllWinner Technology Co., Ltd

Design Name: **A100_B3_AXP707_LPDDR3**

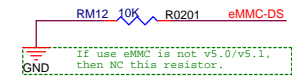
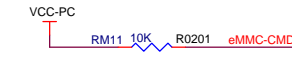
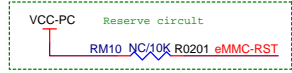
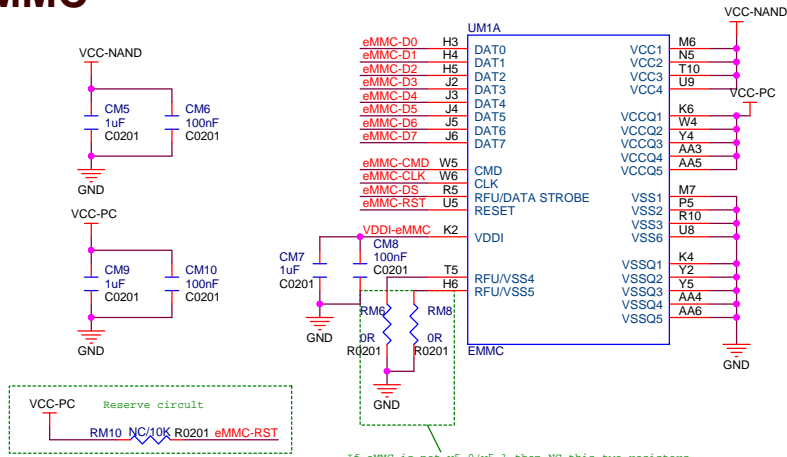
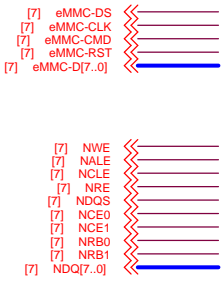
Size: **08 LPDDR3**

Customer: **08 LPDDR3**

Date: **Tuesday, July 14, 2020**

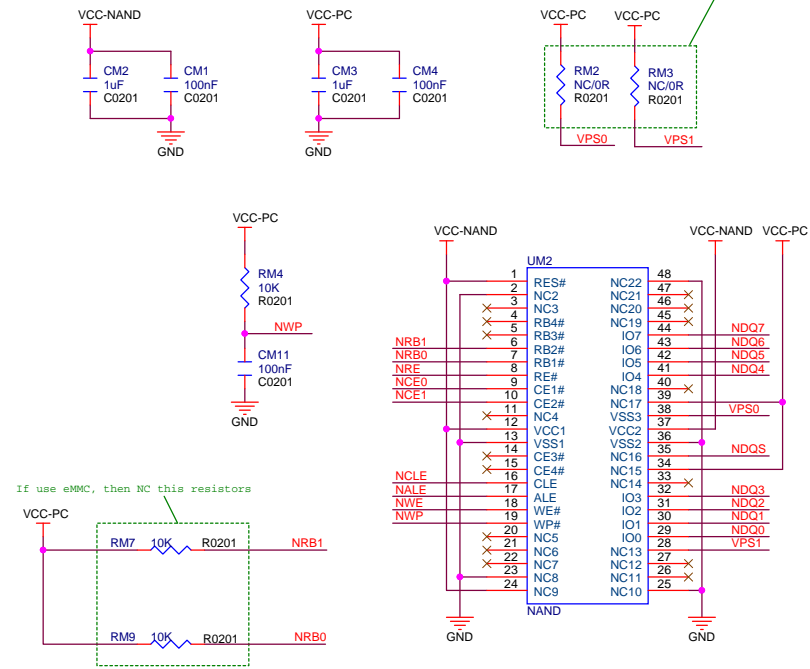
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EMMC



If eMMC is not v5.0/v5.1, then NC this two resistors.

NAND

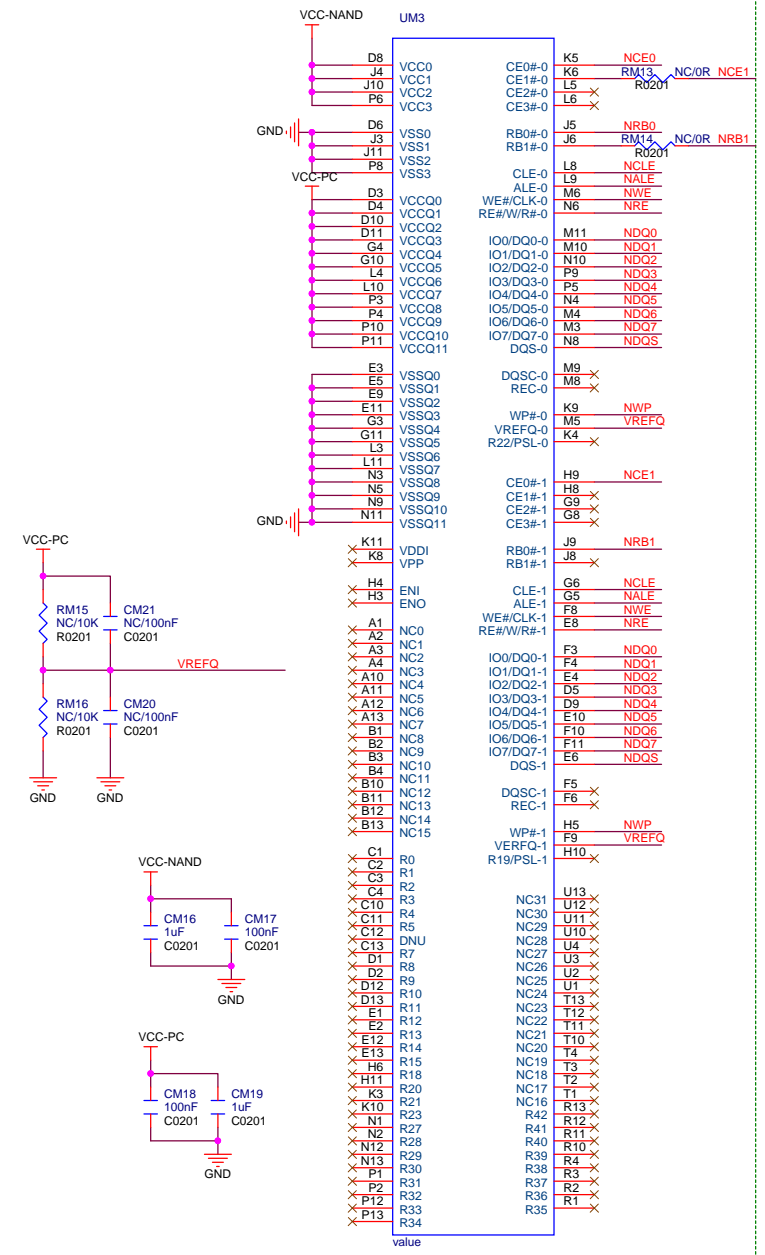


If use eMMC, then NC this resistors

If use Sandisk and Toshiba NAND Flash, mount these two resistor

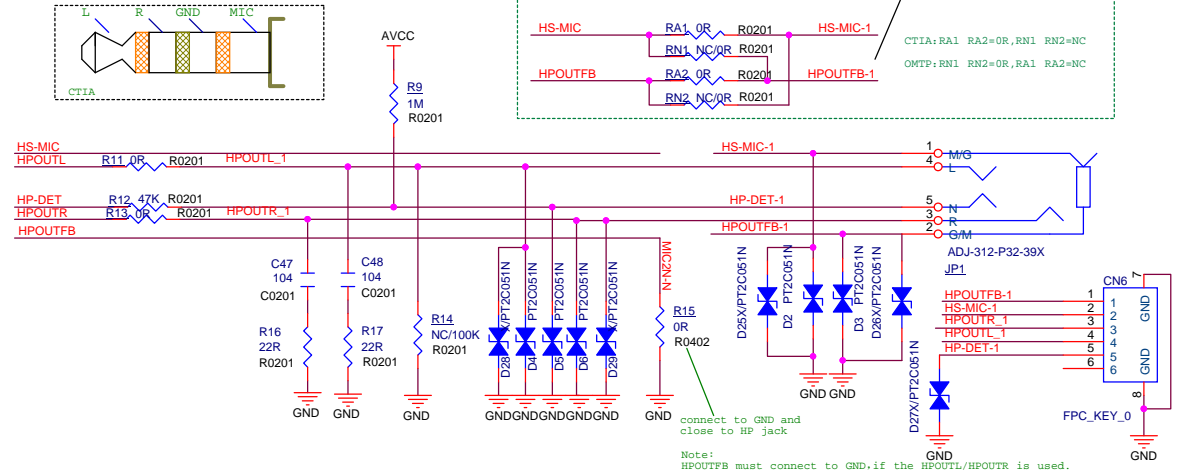
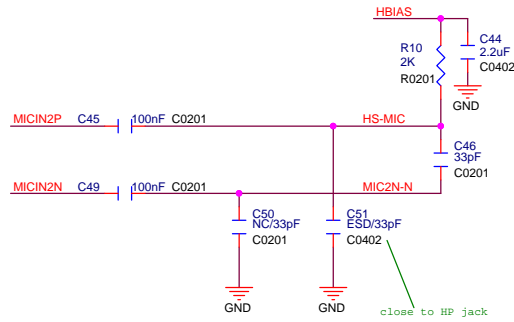
Option: BGA152

Compatible BGA132



HEADPHONE

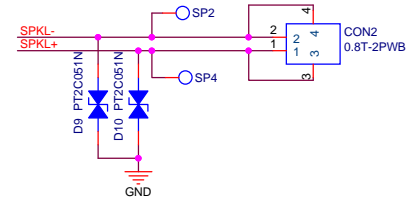
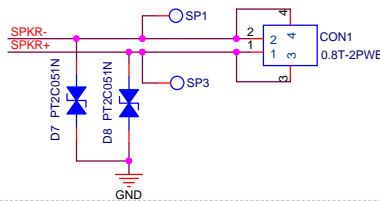
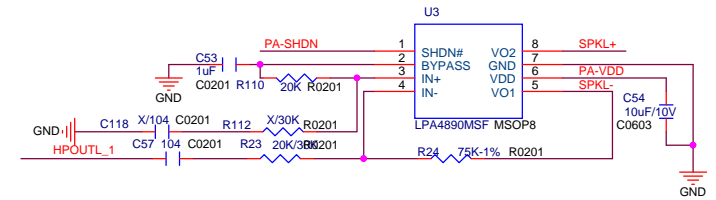
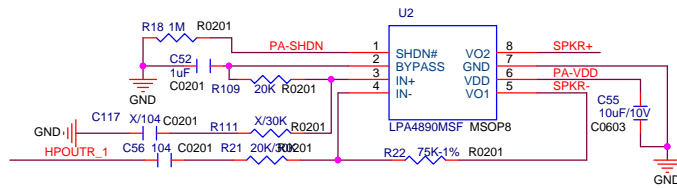
- [6] MICIN1P
- [6] MICIN1N
- [6] MICIN2P
- [6] MICIN2N
- [6] MBIAS
- [6] HBIAS
- [6] HPOUTR
- [6] HPOUTL
- [6] HP-DET
- [6] HS-MIC
- [6] HPOUTFB
- [7] PA-SHDN
- [18] HPOUTR_1
- [18] HPOUTL_1
- [18] HPOUTFB_1



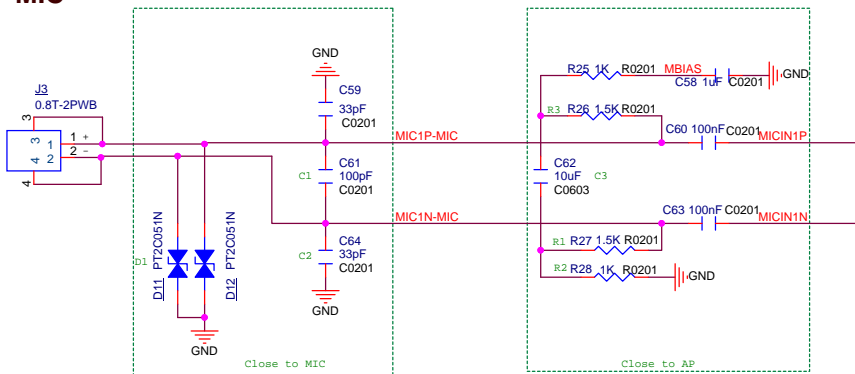
SPEAKER

Default:R-OUT,SINGLE,SPEAKER

- VCC-5V 1A
- AVCC 15mA



MIC



Component	Diferential	single-ended
R1 R2 C1 C3 D1	USE	NC
C2	33pF	0R
R3	1.5K	1K



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SD CARD

- [7] SDC0-D1
- [7] SDC0-D0
- [7] SDC0-CLK
- [7] SDC0-CMD
- [7] SDC0-D3
- [7] SDC0-D2
- [7] SDC0-DET

VCC-CARD
IMAX=0.8A

VCC-IO
1mA

- [5,6] USB0-DM
- [5,6] USB0-DP
- [6] USB1-DM
- [6] USB1-DP

- [7] KD-EINT
- [7] USB0-ID-SOC
- [7] USB1-DRVVBUS

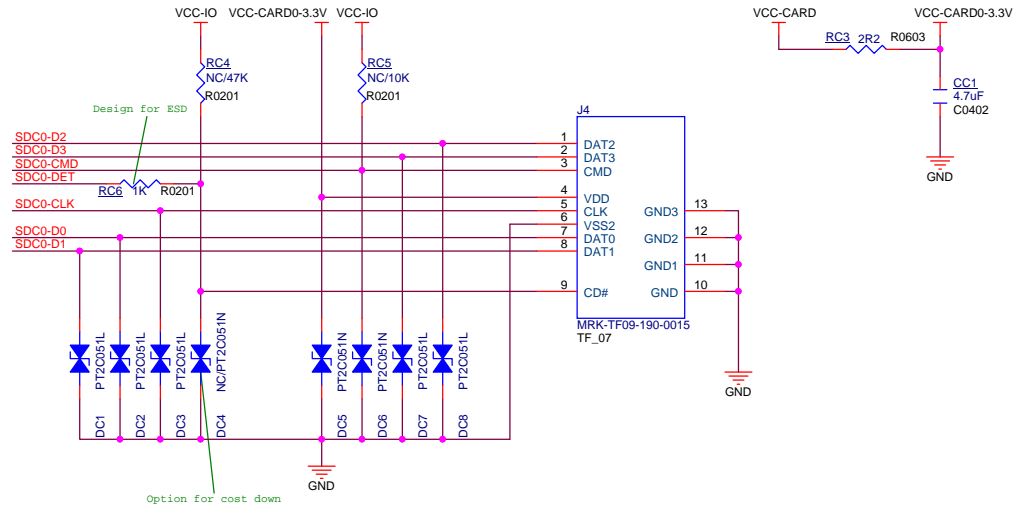
VBUS

VCC-5V

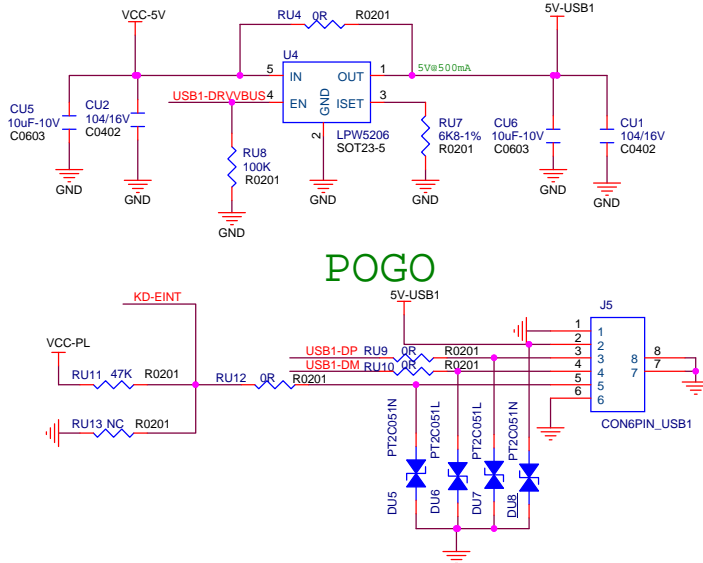
VCC-PL
10mA

VCC-IO
1mA

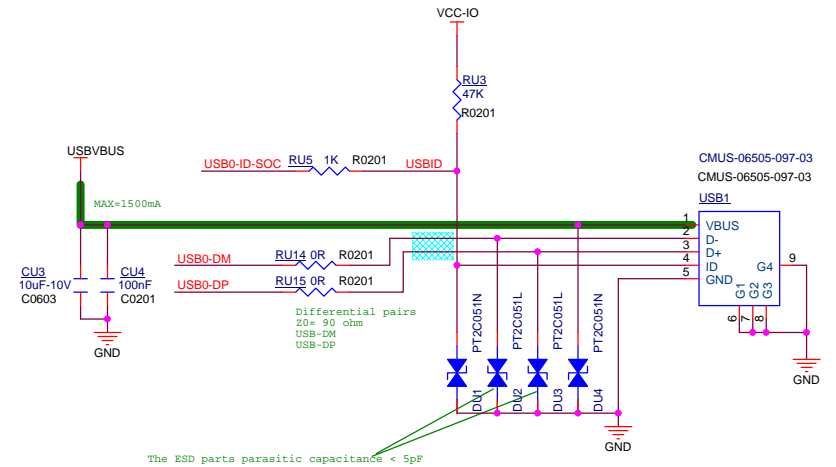
VBUS 2A USBVBUS



USB



POGO



NOTE:
Make sure the routing between the ESD and the USB connectors should be on the same PCB side

[6] MCSIA-CLKN
[6] MCSIA-CLKP

[6] MCSIA-D3N
[6] MCSIA-D3P
[6] MCSIA-D2N
[6] MCSIA-D2P
[6] MCSIA-D1N
[6] MCSIA-D1P
[6] MCSIA-D0N
[6] MCSIA-D0P

[6] MCSIB-CLKN
[6] MCSIB-CLKP
[6] MCSIB-D0N
[6] MCSIB-D0P
[6] MCSIB-D1N
[6] MCSIB-D1P

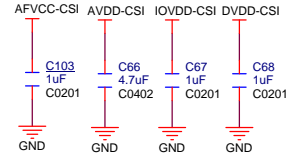
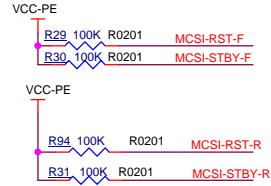
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[7] MCSI-SCK
[7] MCSI-SDA

[7] MCSI-STBY-F
[7] MCSI-STBY-R
[7] MCSI-RST-R

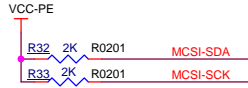
[7] LED-EN

MCSIA-D0[P/N]
MCSIA-D1[P/N]
MCSIA-D2[P/N]
MCSIA-D3[P/N]
MCSIA-CLK[P/N]
Differential pairs
Z0= 100 ohm

MCSIB-D0[P/N]
MCSIB-D1[P/N]
MCSIB-CLK[P/N]
Differential pairs
Z0= 100 ohm

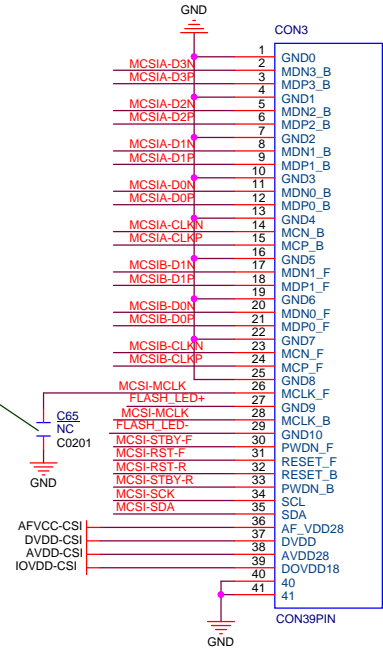
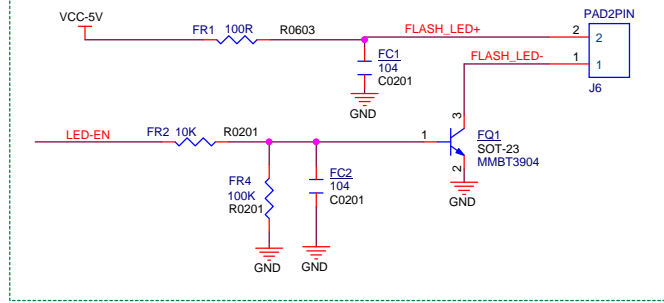


NOTE:
1.The working voltage and current of power need determine according to the peripheral specification.
2.AFVCC-CSI has timing requirements, don't share the same power with DOVDD-CSI.
3.The front and rear cameras need to consider the compatibility of DVDD-CSI voltage.



- VBAT 100mA
- VCC-PL 10mA
- AVDD-CSI 2.8V@30mA
- IOVDD-CSI 1.8V@20mA
- DVDD-CSI 1.2V@25mA
- VCC-PE 10mA
- AFVCC-CSI 2.8V@100mA

FLASH_LED



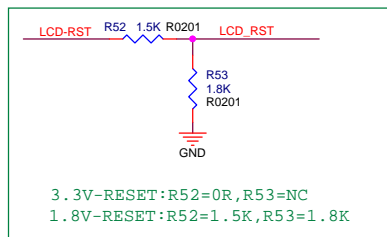
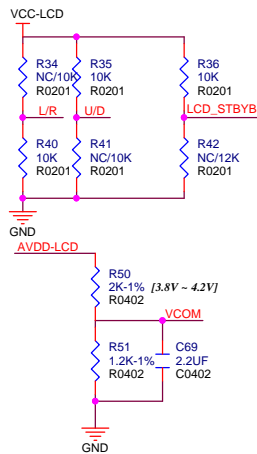
NOTE:
Close to connector.



Allwinner Technology Co.,Ltd		
Design Name	A100_B3_AXP707_LPDDR3	
Size	Page Name	Rev
A3	12 CAMERA	
Date:	Wednesday, June 10, 2020	Sheet 12 of 18

- [7] LCD-D2 MIPI-DSIO-DP0
- [7] LCD-D3 MIPI-DSIO-DM0
- [7] LCD-D4 MIPI-DSIO-DP1
- [7] LCD-D5 MIPI-DSIO-DM1
- [7] LCD-D6 MIPI-DSIO-CKP
- [7] LCD-D7 MIPI-DSIO-CKM
- [7] LCD-D10 MIPI-DSIO-DP2
- [7] LCD-D11 MIPI-DSIO-DM2
- [7] LCD-D12 MIPI-DSIO-DP3
- [7] LCD-D13 MIPI-DSIO-DM3
- [7] LCD-RST LCD-RST
- [7] LCD-PWM LCD-PWM
- [7] LCD-BL-EN LCD-BL-EN
- [7,14] TWIO-SCK TP-SCK
- [7,14] TWIO-SDA TP-SDA
- [7,14] CTP-INT TP-INT
- [7,14] CTP-RST TP-RST

LCD

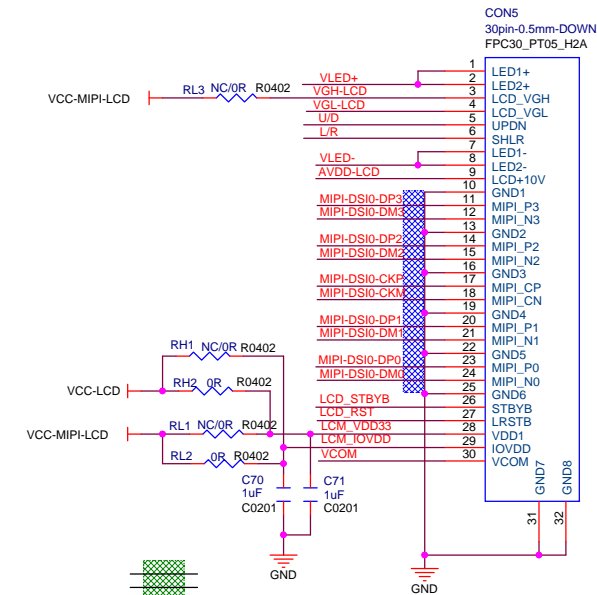
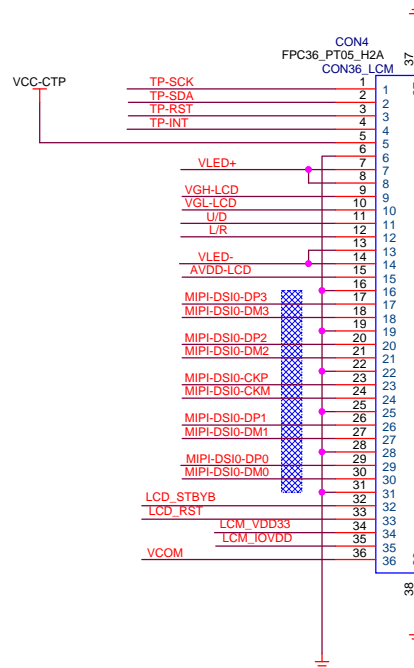


VCC-CTP
I_{MAX}=50mA

VCC-LCD
I_{MAX}=0.2A

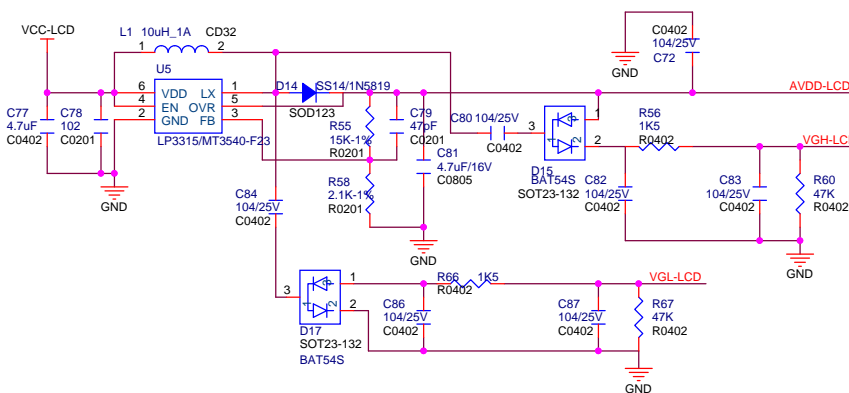
PS
I_{MAX}=0.5A

VCC-MIPH-LCD
I_{MAX}=0.2A

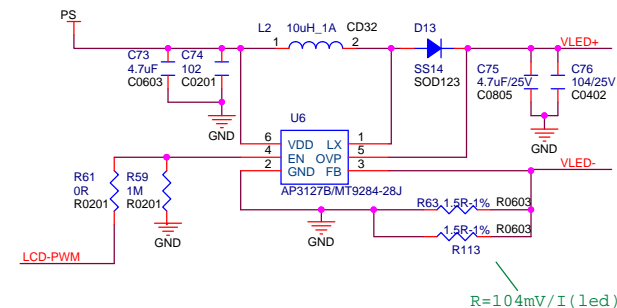


Differential pairs
Z0= 100 ohm

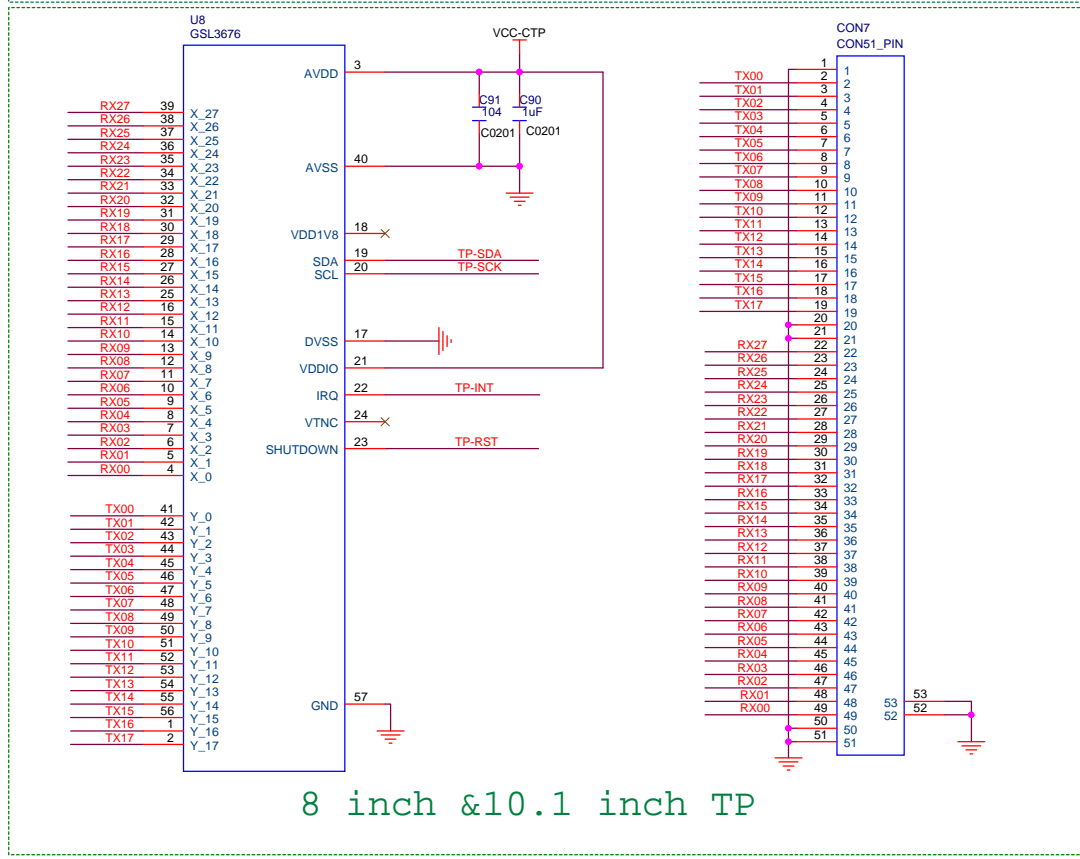
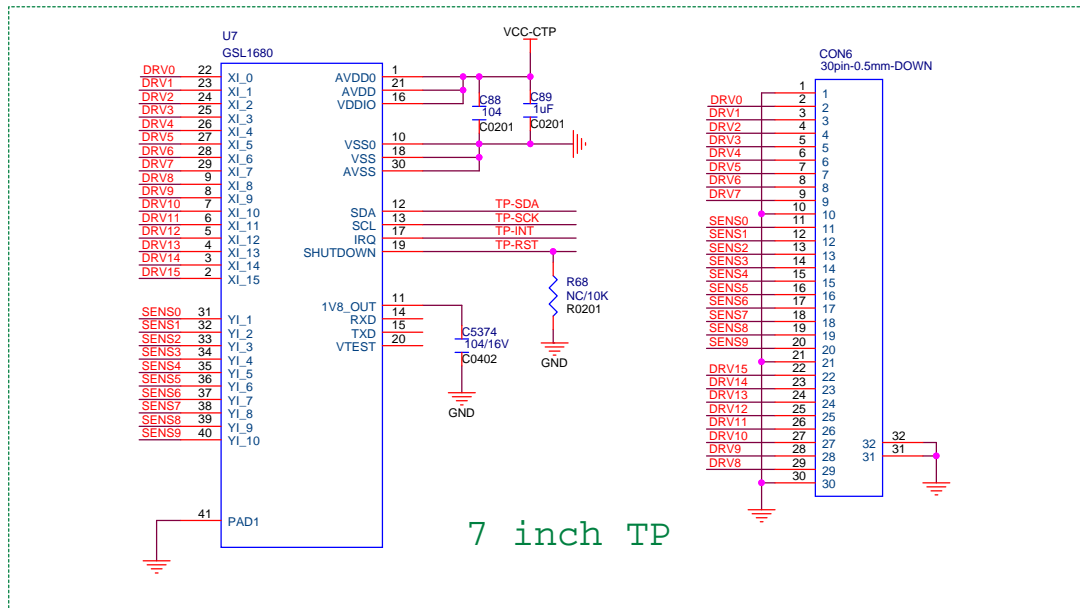
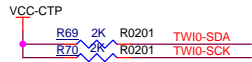
LCD POWER



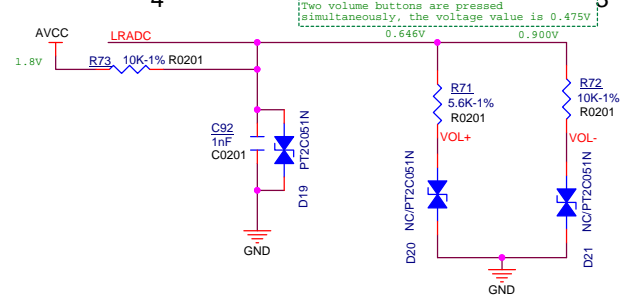
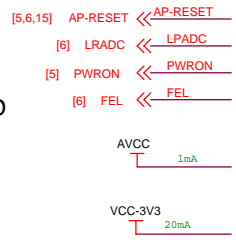
BACKLIGHT



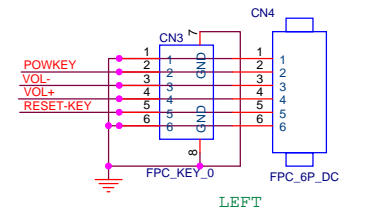
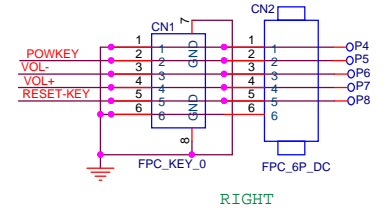
CTP



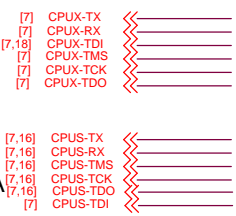
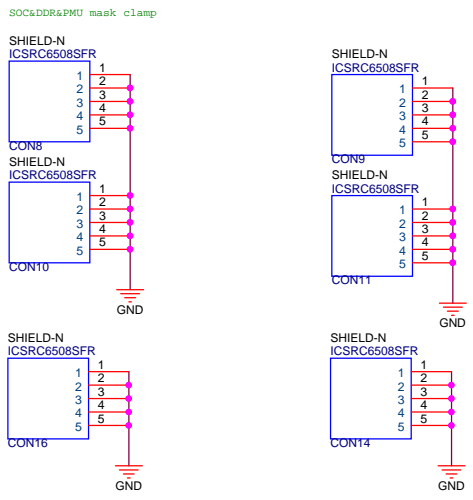
KEY



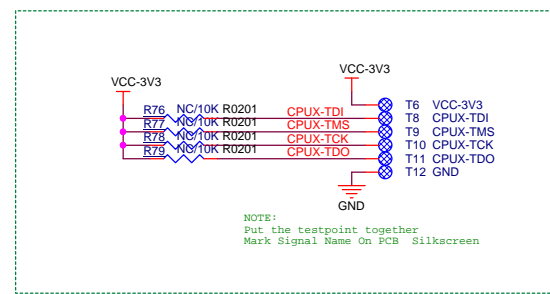
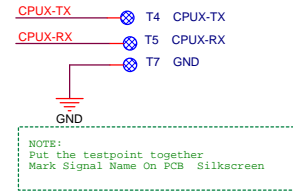
NOTE:
Put the testpoint together
Mark Signal Name On PCB Silkscreen



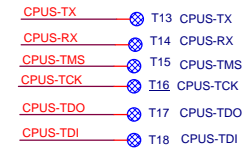
SHIELD



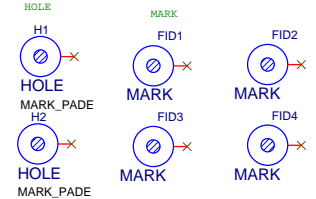
CPUX DEBUG



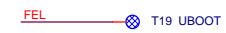
CPUS DEBUG



ASSEMBLE



FEL

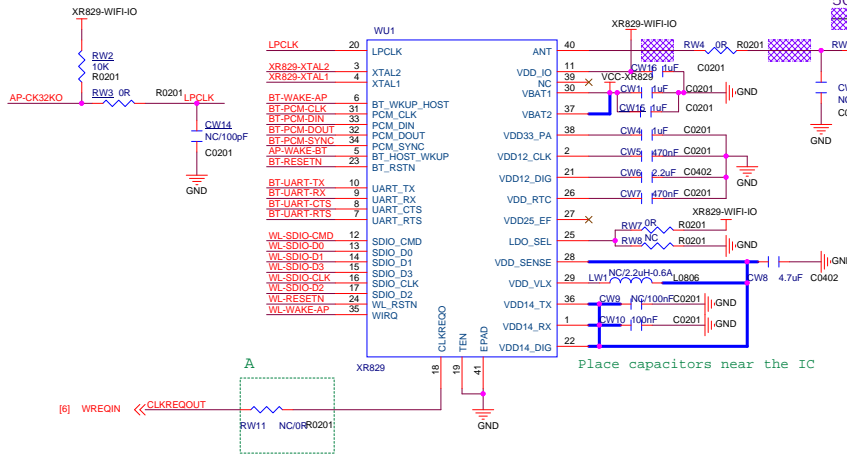
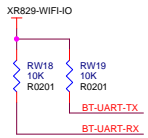
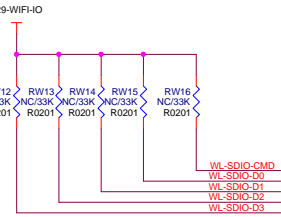
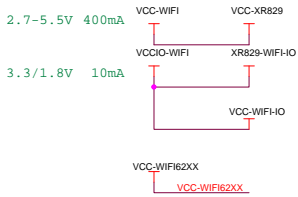


- [7] WL-SDIO-CMD << WL-SDIO-CMD
- [7] WL-SDIO-D0 << WL-SDIO-D0
- [7] WL-SDIO-D1 << WL-SDIO-D1
- [7] WL-SDIO-D2 << WL-SDIO-D2
- [7] WL-SDIO-D3 << WL-SDIO-D3
- [7] WL-SDIO-CLK << WL-SDIO-CLK

- [7.15] WL-PMU-EN << WL-RESETN
- [7.15] WL-WAKE-AP << WL-WAKE-AP

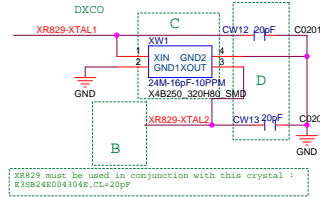
- [7.15] BT-WAKE-AP << BT-WAKE-AP
- [7] BT-PCM-CLK << BT-PCM-CLK
- [7] BT-PCM-DIN << BT-PCM-DIN
- [7] BT-PCM-DOUT << BT-PCM-DOUT
- [7] BT-PCM-SYNC << BT-PCM-SYNC
- [7.15] AP-WAKE-BT << AP-WAKE-BT
- [7.15] BT-RST-N << BT-RST-N

- [7] BT-UART-TX << BT-UART-TX
- [7] BT-UART-RX << BT-UART-RX
- [7] BT-UART-RTS << BT-UART-RTS
- [7] BT-UART-CTS << BT-UART-CTS
- [7] BT-UART-GTS << BT-UART-GTS
- [6] AP-CK32K-OUT << AP-CK32K

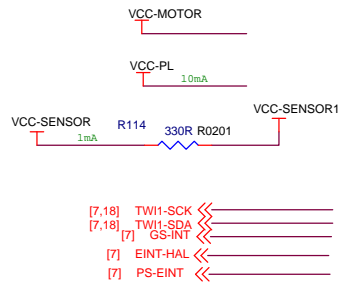


NOTE:

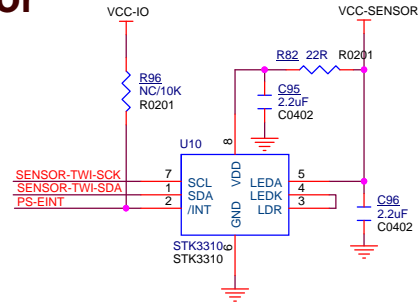
XR829 24M Crystal source	A	B	C	D
Crystal	NC	NC	24M-16pF-10PPM	CW12=20pF, CW13=20pF
DCXO-RFCLK	OR	OR	NC	CW12=0R, CW13=NC



XR829 must be used in conjunction with this crystal :
 83892480041948, CL=20pF

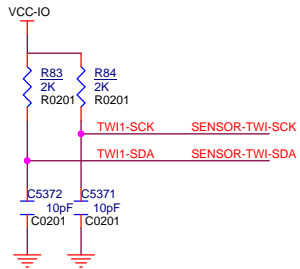
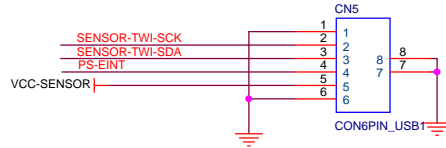


ALS Sensor



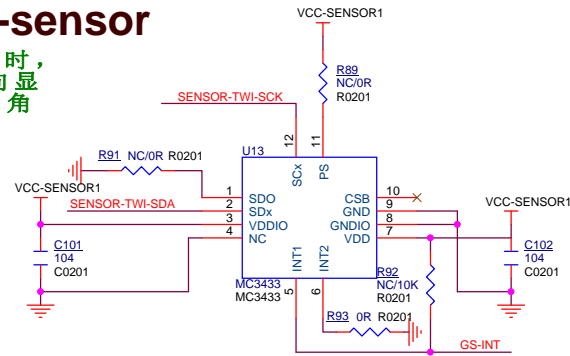
I2C Address: 0x48

ALS Sensor CON

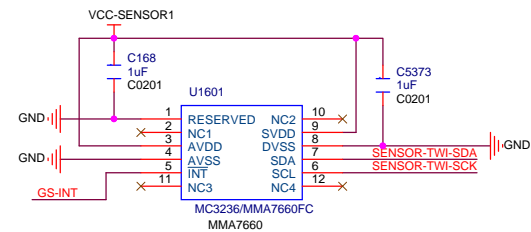


3axis G-sensor

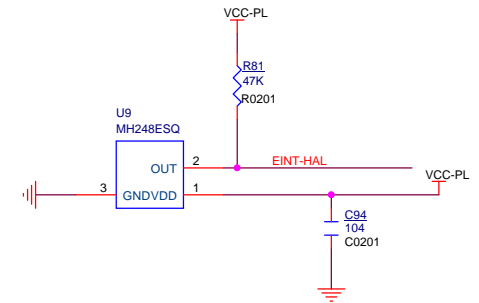
正视显示屏时,
第一PIN朝向显
示屏的左上角



I2C Address: 0x19



Hall switch



Motor

