VERSION HISTORY

M81Q8 Circuit diagram

Index:

Revision	Description	Date	Drawn	Checked	Approved
Ver 1.0	Releas version	2019-12-20	LQS		

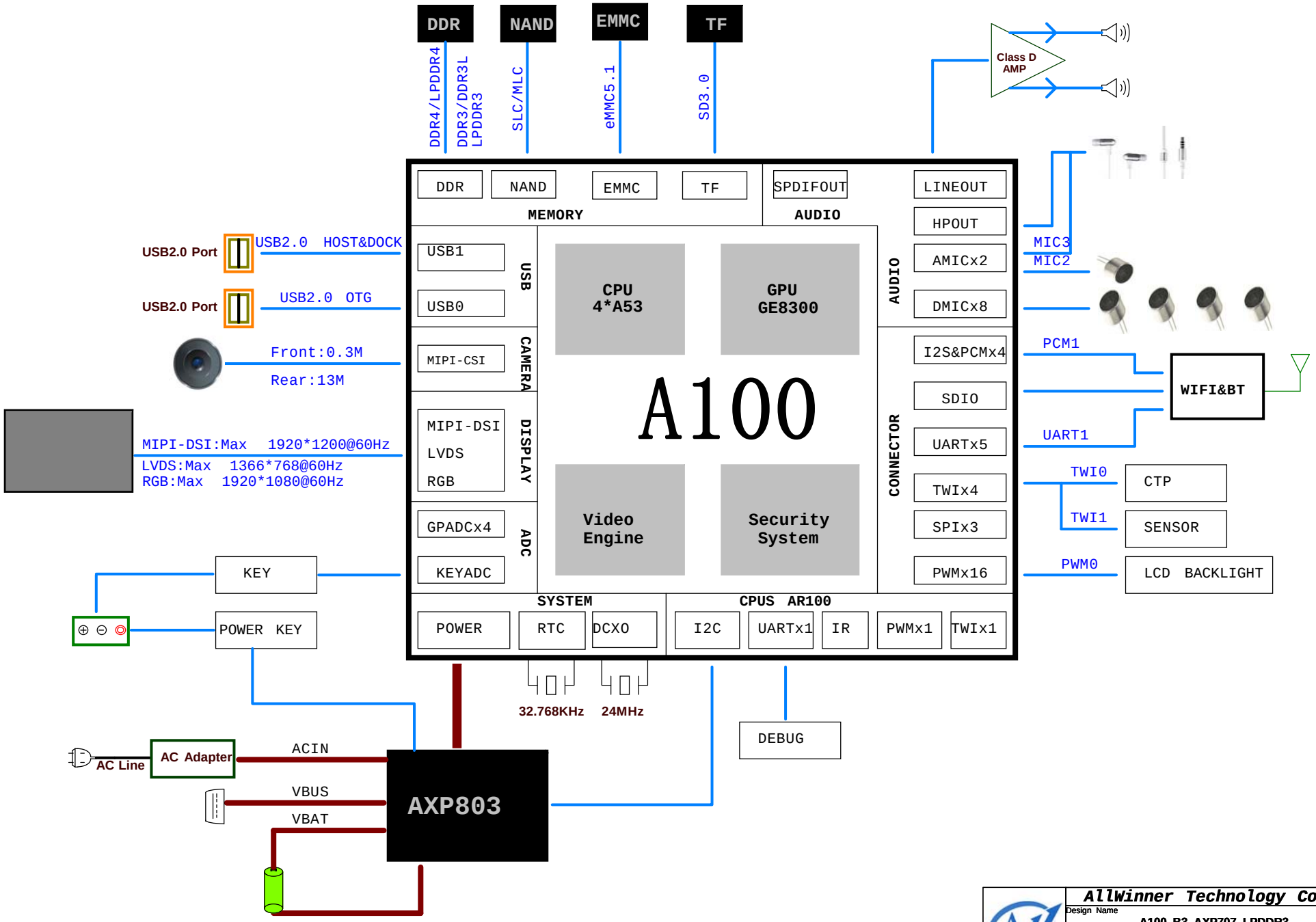
AllWinner Technology Co.,Ltd

Design Name: A100_B3_AXP707_LPDDR3

Size: A3 | Page Name: 01 VERSION HISTORY | Rev:

Date: Saturday, April 25, 2020 | Sheet 1 of 18

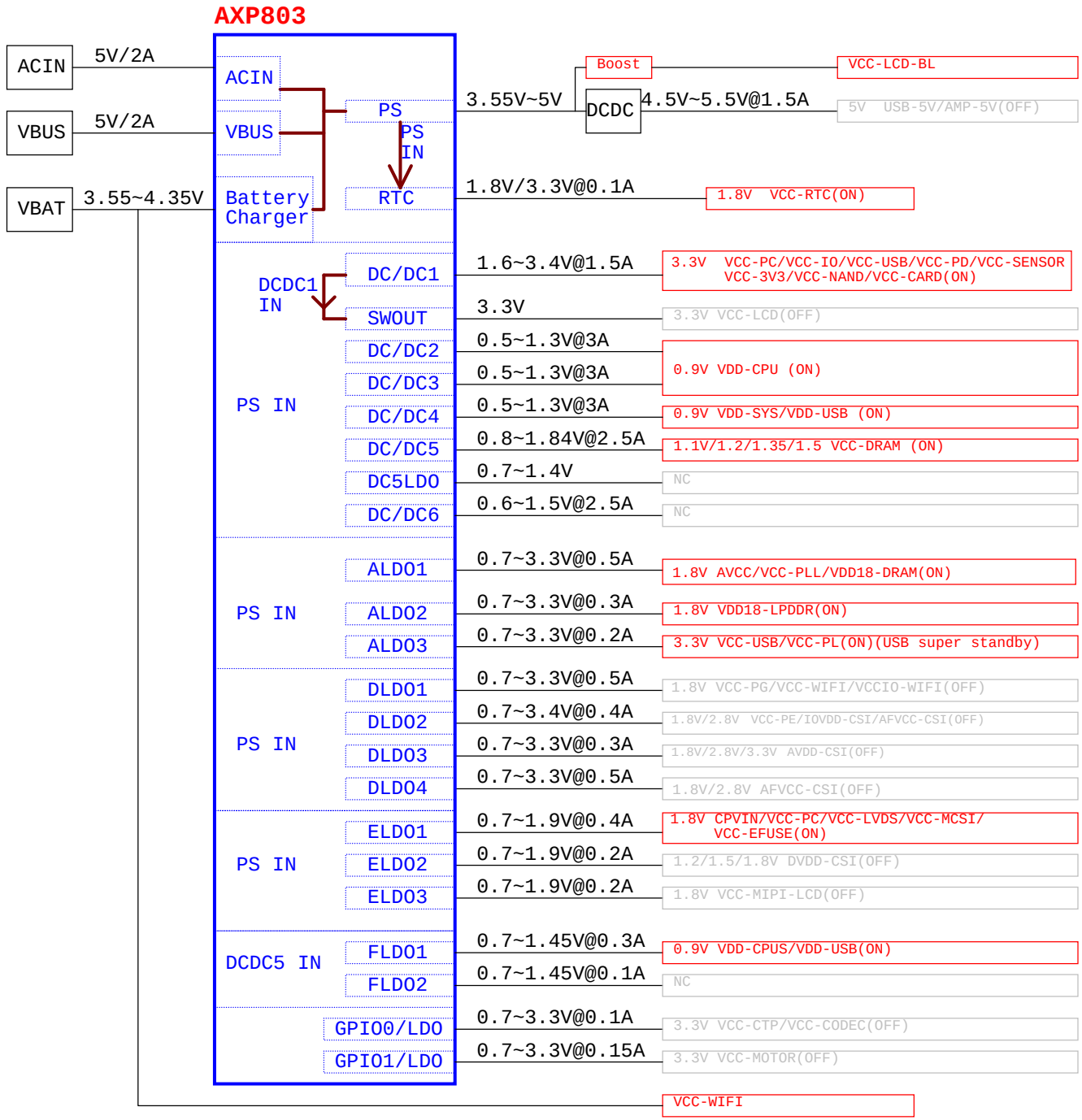
BLOCK



AllWinner Technology Co.,Ltd		
Design Name: A100_B3_AXP707_LPDDR3		
Size: A3	Page Name: 02 BLOCK DIAGRAM	Rev
Date: Saturday, April 25, 2020	Sheet 2 of 18	

DEFAULT POWER ON

DEFAULT POWER OFF



AllWinner Technology Co.,Ltd	
Design Name	A100_B3_AXP707_LPDDR3
Size A3 / Page Name	03 POWER TREE
Rev	
Date: Saturday, April 25, 2020	Sheet 3 of 18

GPIO ASSIGNMENT

PIN	Define	CFG	Function
PB0	CPUX_TMS	4	DEBUG
PB1	CPUX_TCK	4	
PB2	CPUX_TDO	4	
PB3	CPUX_TDI/IRQ-AUDIO	4	
PB4	I2S0-MCLK		GPIO
PB5	I2S0-BCLK		
PB6	I2S0-LRCK		
PB7	I2S0-DOUT		
PB8	LCD-BL-EN	3	
PB9	CPUX_TX	2	DEBUG
PB10	CPUX_RX	2	

PIN	Define	CFG	Function
PE0	MCSI_MCLK	2	CSI
PE1	MCSI_SCK	2	
PE2	MCSI_SDA	2	
PE3			
PE4			
PE5			
PE6	MCSIB_STBY_F	1	
PE7	MCSIB_RST_F	1	
PE8	MCSIA_STBY_R	1	
PE9	MCSIA_RST_R	1	

PIN	Define	CFG	Function
PH0	TWI0_SCK	2	TWI
PH1	TWI0_SDA	2	
PH2	TWI1_SCK	2	
PH3	TWI1_SDA	2	
PH4	PS-EINT	1	GPIO
PH5			
PH6	PA_SHDN	0	
PH7			
PH8	USB0_ID_SOC	0	
PH9	CTP_INT	0	
PH10	CTP_RST	1	
PH11	GS-INT	0	
PH12			
PH13			
PH14			
PH15			
PH16			
PH17			
PH18			
PH19			

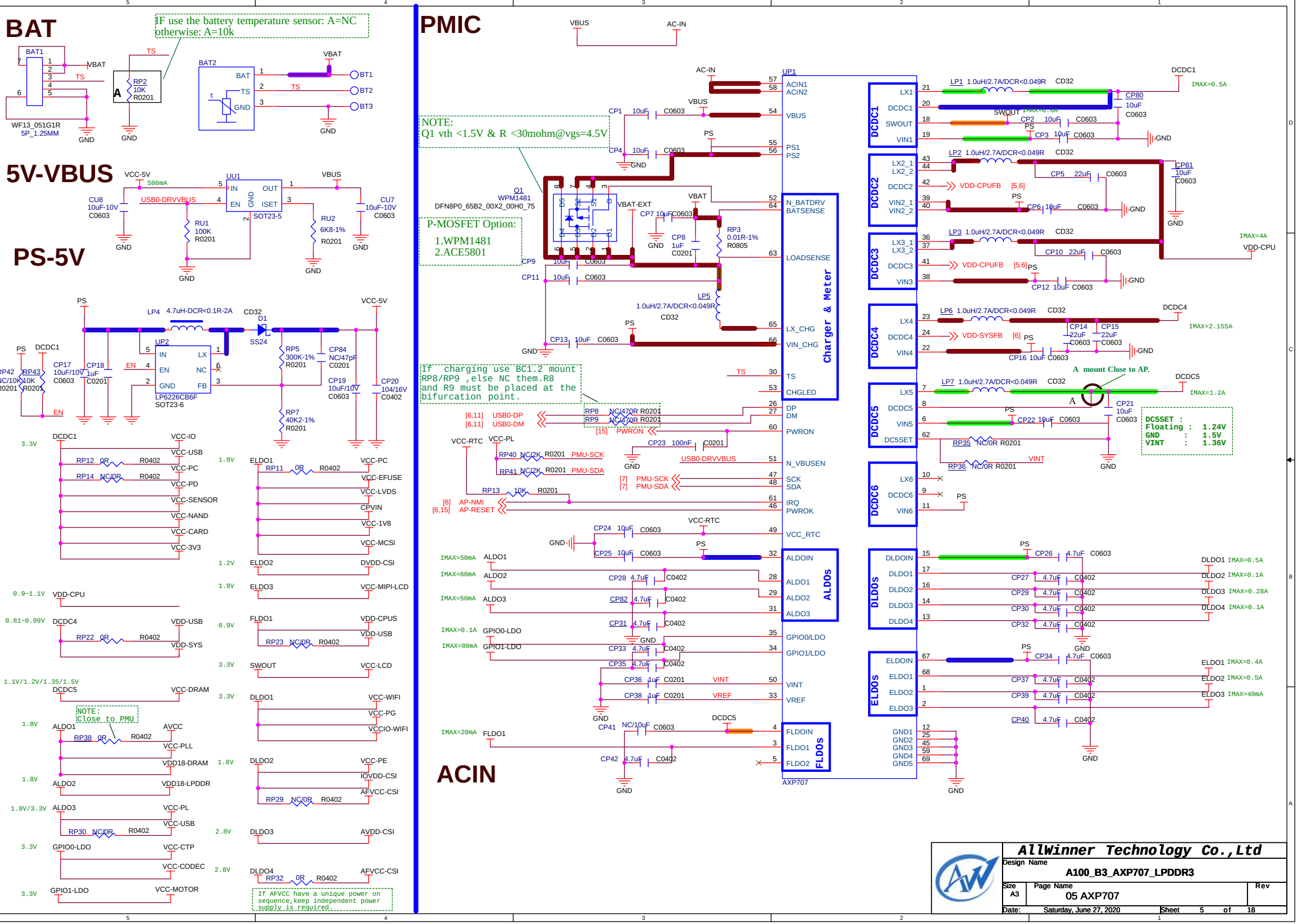
PIN	Define	CFG	Function
PC0	NAND_WE/SDC2_DS	2/3	NAND/eMMC
PC1	NAND_ALE/SDC2_RST	2/3	
PC2	NAND_CLE	2	
PC3	NAND_CE1	2	
PC4	NAND_CE0	2	
PC5	NAND_RE/SDC2_CLK	2/3	
PC6	NAND_RB0/SDC2_CMD	2/3	
PC7	NAND_RB1	2	
PC8	NAND_DQ7/SDC2_D3	2/3	
PC9	NAND_DQ6/SDC2_D4	2/3	
PC10	NAND_DQ5/SDC2_D0	2/3	
PC11	NAND_DQ4/SDC2_D5	2/3	
PC12	NAND_DQS	2	
PC13	NAND_DQ3/SDC2_D1	2/3	
PC14	NAND_DQ2/SDC2_D6	2/3	
PC15	NAND_DQ1/SDC2_D2	2/3	
PC16	NAND_DQ0/SDC2_D7	2/3	

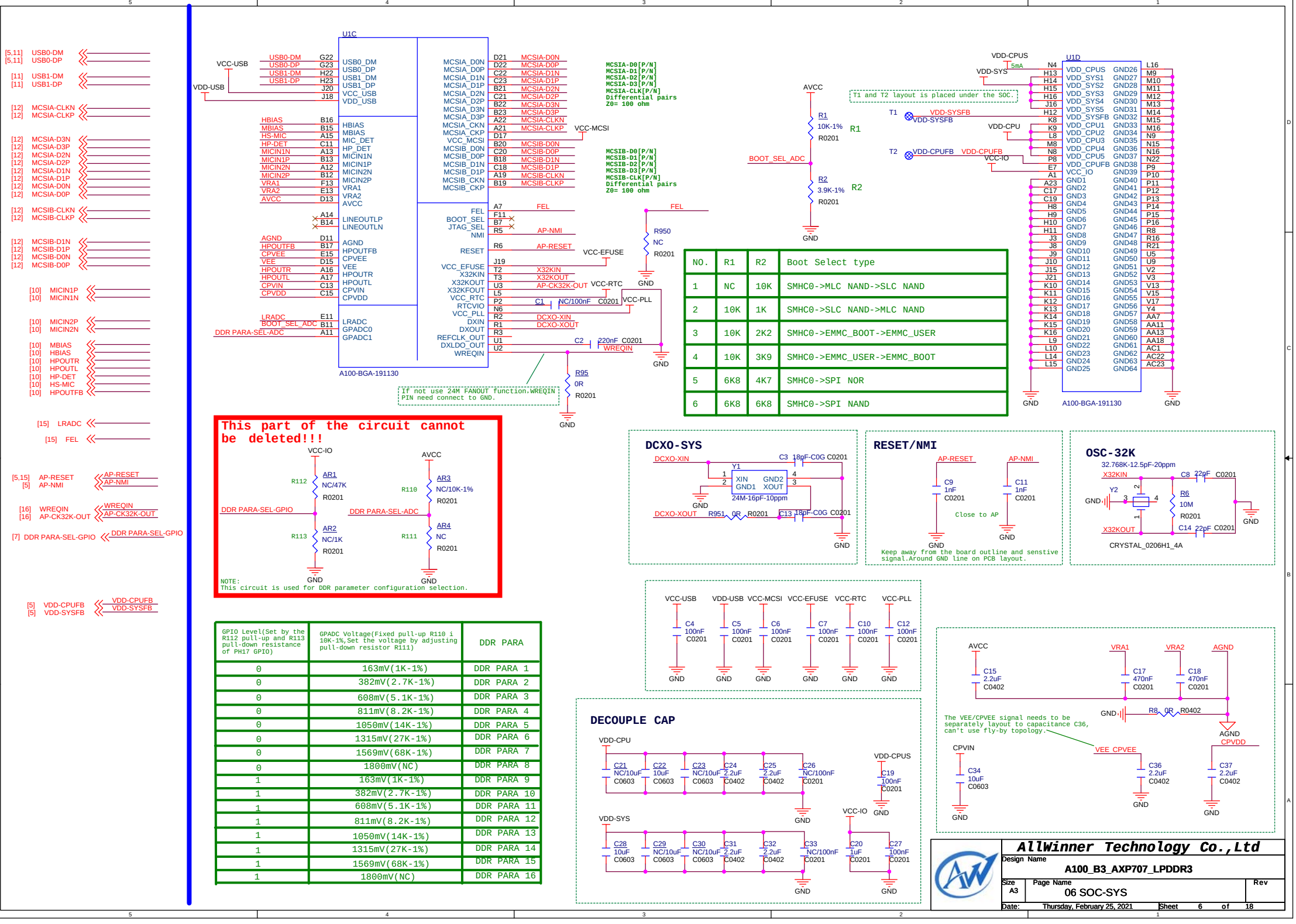
PIN	Define	CFG	Function
PF0	SDC0_D1	2	CARD
PF1	SDC0_D0	2	
PF2	SDC0_CLK	2	
PF3	SDC0_CMD	2	
PF4	SDC0_D3	2	
PF5	SDC0_D2	2	
PF6	SDC0_DET	0	

PIN	Define	CFG	Function
PL0	PMU_SCK	2	CPUS
PL1	PMU_SDA	2	
PL2	BT_RST_N	1	
PL3	BT_WAKE_AP	0	
PL4	AP_WAKE_BT	1	
PL5	WL_PMU_EN	1	
PL6	WL_WAKE_AP	0	
PL7	CPUS-TDI		
PL8	USB1-DRVVBUS		
PL9	EINT-HAL		
PL10	KD-EINT		
PL11	LED-EN	3	

PIN	Define	CFG	Function
PD0	LCD_D2	2	LCD
PD1	LCD_D3	2	
PD2	LCD_D4	2	
PD3	LCD_D5	2	
PD4	LCD_D6	2	
PD5	LCD_D7	2	
PD6	LCD_D10	2	
PD7	LCD_D11	2	
PD8	LCD_D12	2	
PD9	LCD_D13	2	
PD10			
PD11			
PD12			
PD13			
PD14			
PD15			
PD16			
PD17			
PD18			
PD19			
PD20			
PD21			
PD22	LCD_RST	1	
PD23	LCD_PWM	3	

PIN	Define	CFG	Function
PG0	WL_SDIO_CLK	2	WIFI/BT
PG1	WL_SDIO_CMD	2	
PG2	WL_SDIO_D0	2	
PG3	WL_SDIO_D1	2	
PG4	WL_SDIO_D2	2	
PG5	WL_SDIO_D3	2	
PG6	BT_UART_RX	2	
PG7	BT_UART_TX	2	
PG8	BT_UART_CTS	2	
PG9	BT_UART_RTS	2	
PG10	BT_PCM_CLK	3	
PG11	BT_PCM_SYNC	3	
PG12	BT_PCM_DIN	3	
PG13	BT_PCM_DOUT	3	

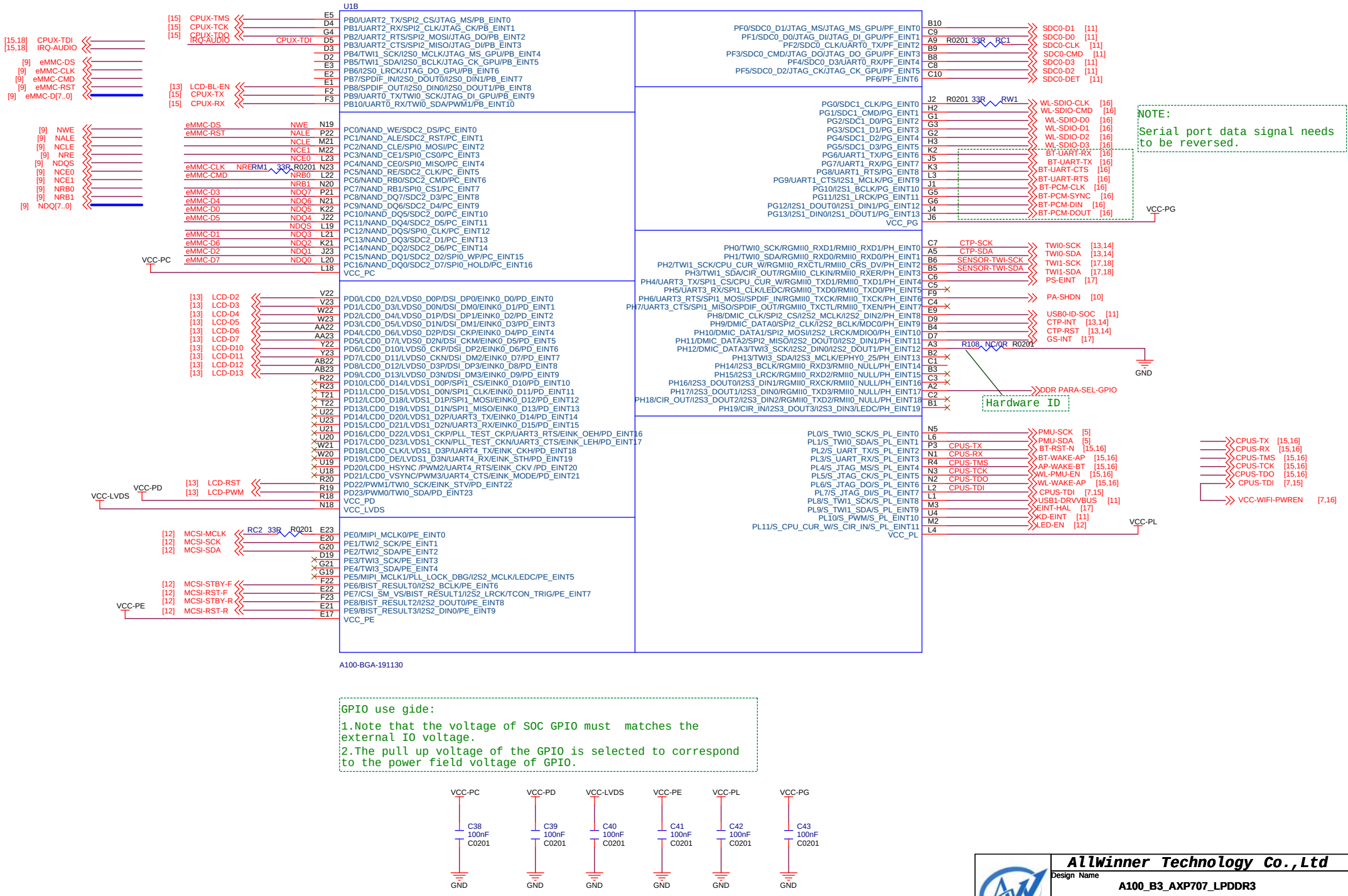

BAT
IF use the battery temperature sensor: A=NC
otherwise: A=10k
BAT1
WF13_051G1R
5P_1.25MM
VBAT
TS
RP2
10K
R0201
BAT2
BT1
BT2
BT3
GND
5V-VBUS
VCC-5V
500mA
UU1
SOT23-5
USB0-DRVVBUS
CU8
10uF-10V
C0603
RU1
100K
R0201
RU2
6K8-1%
CU7
PS-5V
LP4 4.7uH-DCR<0.1R-2A
CD32
D1
SS24
UP2
LP6226CB6F
SOT23-6
CP17
CP18
CP84
NC/47pF
C0201
CP19
10uF/10V
CP20
104/16V
C0402
RP5
300K-1%
RP7
40K2-1%
RP42
RP43
NC/10K
10K
EN
DCDC1
3.3V
VCC-IO
VCC-USB
VCC-PC
VCC-PD
VCC-SENSOR
VCC-NAND
VCC-CARD
VCC-3V3
RP12 0R R0402
RP14 NC/0R R0402
0.9~1.1V
VDD-CPU
0.81~0.99V
DCDC4
VDD-USB
VDD-SYS
RP22 0R R0402
1.1V/1.2V/1.35/1.5V
DCDC5
VCC-DRAM
NOTE:
Close to PMU
1.8V
ALDO1
AVCC
VCC-PLL
VDD18-DRAM
RP38 0R R0402
ALDO2
VDD18-LPDDR
1.8V/3.3V
ALDO3
VCC-PL
VCC-USB
RP30 NC/0R R0402
3.3V
GPIO0-LDO
VCC-CTP
VCC-CODEC
GPIO1-LDO
VCC-MOTOR
1.8V
ELDO1
VCC-PC
VCC-EFUSE
VCC-LVDS
CPVIN
VCC-1V8
VCC-MCSI
RP11 0R R0402
1.2V
ELDO2
DVDD-CSI
ELDO3
VCC-MIPI-LCD
0.9V
FLDO1
VDD-CPUS
VDD-USB
RP23 NC/0R R0402
SWOUT
VCC-LCD
DLDO1
VCC-WIFI
VCC-PG
VCCIO-WIFI
DLDO2
VCC-PE
IOVDD-CSI
AFVCC-CSI
RP29 NC/0R R0402
2.8V
DLDO3
AVDD-CSI
DLDO4
AFVCC-CSI
RP32 0R R0402
If AFVCC have a unique power on sequence,keep independent power supply is required.
PMIC
VBUS
AC-IN
UP1
ACIN1
ACIN2
VBUS
PS1
PS2
NOTE:
Q1 vth <1.5V & R <30mohm@vgs=4.5V
Q1
WPM1481
DFN8P0_65B2_00X2_00H0_75
P-MOSFET Option:
1.WPM1481
2.ACE5801
VBAT-EXT
CP7 10uF C0603
CP8 1uF C0201
RP3 0.01R-1% R0805
CP9 10uF C0603
CP11 10uF C0603
LP5 1.0uH/2.7A/DCR<0.049R
CP13 10uF C0603
N_BATDRV
BATSENSE
LOADSENSE
LX_CHG
VIN_CHG
Charger & Meter
If charging use BC1.2 mount RP8/RP9 ,else NC them.R8 and R9 must be placed at the bifurcation point.
TS
CHGLED
[6,11] USB0-DP
[6,11] USB0-DM
RP8 NC/470R R0201
RP9 NC/470R R0201
DP
DM
[15] PWRON
PWRON
VCC-RTC
VCC-PL
RP40 NC/2K R0201 PMU-SCK
RP41 NC/2K R0201 PMU-SDA
CP23 100nF C0201
USB0-DRVVBUS
N_VBUSEN
[7] PMU-SCK
[7] PMU-SDA
SCK
SDA
RP13 10K R0201
[6] AP-NMI
[6,15] AP-RESET
IRQ
PWROK
VCC_RTC
CP24 10uF C0603
CP25 10uF C0603
IMAX=50mA ALDO1
IMAX=60mA ALDO2
IMAX=50mA ALDO3
CP28 4.7uF C0402
CP82 4.7uF C0402
CP31 4.7uF C0402
ALDOIN
ALDO1
ALDO2
ALDO3
ALDOs
IMAX=0.1A GPIO0-LDO
IMAX=80mA GPIO1-LDO
CP33 4.7uF C0402
CP35 4.7uF C0402
GPIO0/LDO
GPIO1/LDO
CP36 1uF C0201
CP38 1uF C0201
VINT
VREF
IMAX=20mA FLDO1
CP41 NC/10uF C0603
CP42 4.7uF C0402
FLDOIN
FLDO1
FLDO2
FLDOs
AXP707
ACIN
DCDC1
LX1
DCDC1
SWOUT
VIN1
LP1 1.0uH/2.7A/DCR<0.049R
CD32
CP80 10uF C0603
IMAX=0.5A
CP2 10uF C0603
CP3 10uF C0603
DCDC2
LX2_1
LX2_2
DCDC2
VIN2_1
VIN2_2
LP2 1.0uH/2.7A/DCR<0.049R
CP81 10uF C0603
CP5 22uF C0603
CP6 10uF C0603
VDD-CPUFB [5,6]
DCDC3
LX3_1
LX3_2
DCDC3
VIN3
LP3 1.0uH/2.7A/DCR<0.049R
IMAX=4A
VDD-CPU
CP10 22uF C0603
CP12 10uF C0603
DCDC4
LX4
DCDC4
VIN4
LP6 1.0uH/2.7A/DCR<0.049R
IMAX=2.155A
VDD-SYSFB [6]
CP14 22uF C0603
CP15 22uF C0603
CP16 10uF C0603
DCDC5
LX5
DCDC5
VIN5
DC5SET
LP7 1.0uH/2.7A/DCR<0.049R
IMAX=1.2A
A mount Close to AP.
CP21 10uF C0603
CP22 10uF C0603
RP35 NC/0R R0201
RP36 NC/0R R0201
VINT
DC5SET :
Floating : 1.24V
GND : 1.5V
VINT : 1.36V
DCDC6
LX6
DCDC6
VIN6
DLDOIN
DLDO1
DLDO2
DLDO3
DLDO4
DLDOs
CP26 4.7uF C0603
CP27 4.7uF C0402
CP29 4.7uF C0402
CP30 4.7uF C0402
CP32 4.7uF C0402
DLDO1 IMAX=0.5A
DLDO2 IMAX=0.1A
DLDO3 IMAX=0.28A
DLDO4 IMAX=0.1A
ELDOIN
ELDO1
ELDO2
ELDO3
ELDOs
CP34 4.7uF C0603
CP37 4.7uF C0402
CP39 4.7uF C0402
CP40 4.7uF C0402
ELDO1 IMAX=0.4A
ELDO2 IMAX=0.5A
ELDO3 IMAX=40mA
GND1
GND2
GND3
GND4
GND5
AllWinner Technology Co.,Ltd
Design Name
A100_B3_AXP707_LPDDR3
Size
A3
Page Name
05 AXP707
Rev
Date: Saturday, June 27, 2020
Sheet 5 of 18



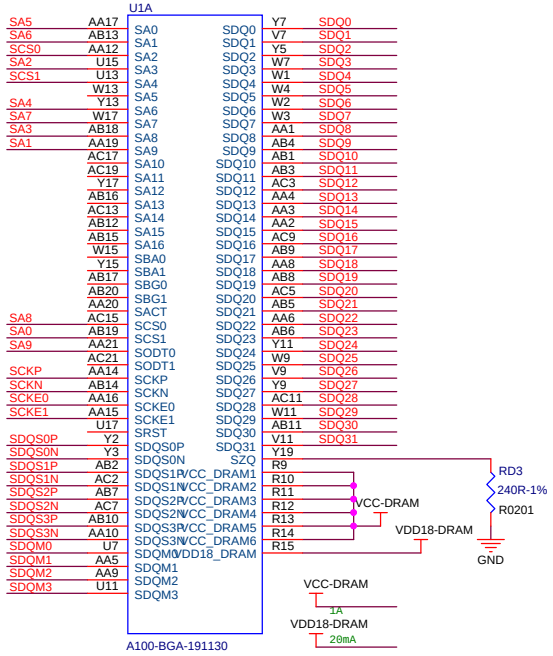
NO.	R1	R2	Boot Select type
1	NC	10K	SMHC0->MLC NAND->SLC NAND
2	10K	1K	SMHC0->SLC NAND->MLC NAND
3	10K	2K2	SMHC0->EMMC_BOOT->EMMC_USER
4	10K	3K9	SMHC0->EMMC_USER->EMMC_BOOT
5	6K8	4K7	SMHC0->SPI NOR
6	6K8	6K8	SMHC0->SPI NAND

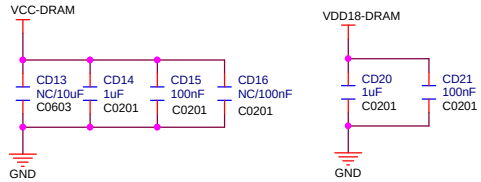
GPIO Level(Set by the R112 pull-up and R113 pull-down resistance of PH17 GPIO)	GPADC Voltage(Fixed pull-up R110 i 10K-1%,Set the voltage by adjusting pull-down resistor R111)	DDR PARA
0	163mV(1K-1%)	DDR PARA 1
0	382mV(2.7K-1%)	DDR PARA 2
0	608mV(5.1K-1%)	DDR PARA 3
0	811mV(8.2K-1%)	DDR PARA 4
0	1050mV(14K-1%)	DDR PARA 5
0	1315mV(27K-1%)	DDR PARA 6
0	1569mV(68K-1%)	DDR PARA 7
0	1800mV(NC)	DDR PARA 8
1	163mV(1K-1%)	DDR PARA 9
1	382mV(2.7K-1%)	DDR PARA 10
1	608mV(5.1K-1%)	DDR PARA 11
1	811mV(8.2K-1%)	DDR PARA 12
1	1050mV(14K-1%)	DDR PARA 13
1	1315mV(27K-1%)	DDR PARA 14
1	1569mV(68K-1%)	DDR PARA 15
1	1800mV(NC)	DDR PARA 16

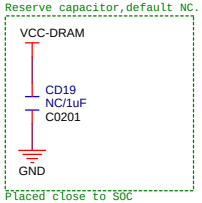
Design Name	AllWinner Technology Co.,Ltd
	A100_B3_AXP707_LPDDR3
Size A3	Page Name 06 SOC-SYS
Rev	
Date: Thursday, February 25, 2021	Sheet 6 of 18


U1B
PB0/UART2_TX/SPI2_CS/JTAG_MS/PB_EINT0
PB1/UART2_RX/SPI2_CLK/JTAG_CK/PB_EINT1
PB2/UART2_RTS/SPI2_MOSI/JTAG_DO/PB_EINT2
PB3/UART2_CTS/SPI2_MISO/JTAG_DI/PB_EINT3
PB4/TWI1_SCK/I2S0_MCLK/JTAG_MS_GPU/PB_EINT4
PB5/TWI1_SDA/I2S0_BCLK/JTAG_CK_GPU/PB_EINT5
PB6/I2S0_LRCK/JTAG_DO_GPU/PB_EINT6
PB7/SPDIF_IN/I2S0_DOUT0/I2S0_DIN1/PB_EINT7
PB8/SPDIF_OUT/I2S0_DIN0/I2S0_DOUT1/PB_EINT8
PB9/UART0_TX/TWI0_SCK/JTAG_DI_GPU/PB_EINT9
PB10/UART0_RX/TWI0_SDA/PWM1/PB_EINT10
PC0/NAND_WE/SDC2_DS/PC_EINT0
PC1/NAND_ALE/SDC2_RST/PC_EINT1
PC2/NAND_CLE/SPI0_MOSI/PC_EINT2
PC3/NAND_CE1/SPI0_CS0/PC_EINT3
PC4/NAND_CE0/SPI0_MISO/PC_EINT4
PC5/NAND_RE/SDC2_CLK/PC_EINT5
PC6/NAND_RB0/SDC2_CMD/PC_EINT6
PC7/NAND_RB1/SPI0_CS1/PC_EINT7
PC8/NAND_DQ7/SDC2_D3/PC_EINT8
PC9/NAND_DQ6/SDC2_D4/PC_EINT9
PC10/NAND_DQ5/SDC2_D0/PC_EINT10
PC11/NAND_DQ4/SDC2_D5/PC_EINT11
PC12/NAND_DQS/SPI0_CLK/PC_EINT12
PC13/NAND_DQ3/SDC2_D1/PC_EINT13
PC14/NAND_DQ2/SDC2_D6/PC_EINT14
PC15/NAND_DQ1/SDC2_D2/SPI0_WP/PC_EINT15
PC16/NAND_DQ0/SDC2_D7/SPI0_HOLD/PC_EINT16
VCC_PC
PD0/LCD0_D2/LVDS0_D0P/DSI_DP0/EINK0_D0/PD_EINT0
PD1/LCD0_D3/LVDS0_D0N/DSI_DM0/EINK0_D1/PD_EINT1
PD2/LCD0_D4/LVDS0_D1P/DSI_DP1/EINK0_D2/PD_EINT2
PD3/LCD0_D5/LVDS0_D1N/DSI_DM1/EINK0_D3/PD_EINT3
PD4/LCD0_D6/LVDS0_D2P/DSI_CKP/EINK0_D4/PD_EINT4
PD5/LCD0_D7/LVDS0_D2N/DSI_CKM/EINK0_D5/PD_EINT5
PD6/LCD0_D10/LVDS0_CKP/DSI_DP2/EINK0_D6/PD_EINT6
PD7/LCD0_D11/LVDS0_CKN/DSI_DM2/EINK0_D7/PD_EINT7
PD8/LCD0_D12/LVDS0_D3P/DSI_DP3/EINK0_D8/PD_EINT8
PD9/LCD0_D13/LVDS0_D3N/DSI_DM3/EINK0_D9/PD_EINT9
PD10/LCD0_D14/LVDS1_D0P/SPI1_CS/EINK0_D10/PD_EINT10
PD11/LCD0_D15/LVDS1_D0N/SPI1_CLK/EINK0_D11/PD_EINT11
PD12/LCD0_D18/LVDS1_D1P/SPI1_MOSI/EINK0_D12/PD_EINT12
PD13/LCD0_D19/LVDS1_D1N/SPI1_MISO/EINK0_D13/PD_EINT13
PD14/LCD0_D20/LVDS1_D2P/UART3_TX/EINK0_D14/PD_EINT14
PD15/LCD0_D21/LVDS1_D2N/UART3_RX/EINK0_D15/PD_EINT15
PD16/LCD0_D22/LVDS1_CKP/PLL_TEST_CKP/UART3_RTS/EINK_OEH/PD_EINT16
PD17/LCD0_D23/LVDS1_CKN/PLL_TEST_CKN/UART3_CTS/EINK_LEH/PD_EINT17
PD18/LCD0_CLK/LVDS1_D3P/UART4_TX/EINK_CKH/PD_EINT18
PD19/LCD0_DE/LVDS1_D3N/UART4_RX/EINK_STH/PD_EINT19
PD20/LCD0_HSYNC /PWM2/UART4_RTS/EINK_CKV /PD_EINT20
PD21/LCD0_VSYNC/PWM3/UART4_CTS/EINK_MODE/PD_EINT21
PD22/PWM1/TWI0_SCK/EINK_STV/PD_EINT22
PD23/PWM0/TWI0_SDA/PD_EINT23
VCC_PD
VCC_LVDS
PE0/MIPI_MCLK0/PE_EINT0
PE1/TWI2_SCK/PE_EINT1
PE2/TWI2_SDA/PE_EINT2
PE3/TWI3_SCK/PE_EINT3
PE4/TWI3_SDA/PE_EINT4
PE5/MIPI_MCLK1/PLL_LOCK_DBG/I2S2_MCLK/LEDC/PE_EINT5
PE6/BIST_RESULT0/I2S2_BCLK/PE_EINT6
PE7/CSI_SM_VS/BIST_RESULT1/I2S2_LRCK/TCON_TRIG/PE_EINT7
PE8/BIST_RESULT2/I2S2_DOUT0/PE_EINT8
PE9/BIST_RESULT3/I2S2_DIN0/PE_EINT9
VCC_PE
PF0/SDC0_D1/JTAG_MS/JTAG_MS_GPU/PF_EINT0
PF1/SDC0_D0/JTAG_DI/JTAG_DI_GPU/PF_EINT1
PF2/SDC0_CLK/UART0_TX/PF_EINT2
PF3/SDC0_CMD/JTAG_DO/JTAG_DO_GPU/PF_EINT3
PF4/SDC0_D3/UART0_RX/PF_EINT4
PF5/SDC0_D2/JTAG_CK/JTAG_CK_GPU/PF_EINT5
PF6/PF_EINT6
PG0/SDC1_CLK/PG_EINT0
PG1/SDC1_CMD/PG_EINT1
PG2/SDC1_D0/PG_EINT2
PG3/SDC1_D1/PG_EINT3
PG4/SDC1_D2/PG_EINT4
PG5/SDC1_D3/PG_EINT5
PG6/UART1_TX/PG_EINT6
PG7/UART1_RX/PG_EINT7
PG8/UART1_RTS/PG_EINT8
PG9/UART1_CTS/I2S1_MCLK/PG_EINT9
PG10/I2S1_BCLK/PG_EINT10
PG11/I2S1_LRCK/PG_EINT11
PG12/I2S1_DOUT0/I2S1_DIN1/PG_EINT12
PG13/I2S1_DIN0/I2S1_DOUT1/PG_EINT13
VCC_PG
PH0/TWI0_SCK/RGMII0_RXD1/RMII0_RXD1/PH_EINT0
PH1/TWI0_SDA/RGMII0_RXD0/RMII0_RXD0/PH_EINT1
PH2/TWI1_SCK/CPU_CUR_W/RGMII0_RXCTL/RMII0_CRS_DV/PH_EINT2
PH3/TWI1_SDA/CIR_OUT/RGMII0_CLKIN/RMII0_RXER/PH_EINT3
PH4/UART3_TX/SPI1_CS/CPU_CUR_W/RGMII0_TXD1/RMII0_TXD1/PH_EINT4
PH5/UART3_RX/SPI1_CLK/LEDC/RGMII0_TXD0/RMII0_TXD0/PH_EINT5
PH6/UART3_RTS/SPI1_MOSI/SPDIF_IN/RGMII0_TXCK/RMII0_TXCK/PH_EINT6
PH7/UART3_CTS/SPI1_MISO/SPDIF_OUT/RGMII0_TXCTL/RMII0_TXEN/PH_EINT7
PH8/DMIC_CLK/SPI2_CS/I2S2_MCLK/I2S2_DIN2/PH_EINT8
PH9/DMIC_DATA0/SPI2_CLK/I2S2_BCLK/MDC0/PH_EINT9
PH10/DMIC_DATA1/SPI2_MOSI/I2S2_LRCK/MDIO0/PH_EINT10
PH11/DMIC_DATA2/SPI2_MISO/I2S2_DOUT0/I2S2_DIN1/PH_EINT11
PH12/DMIC_DATA3/TWI3_SCK/I2S2_DIN0/I2S2_DOUT1/PH_EINT12
PH13/TWI3_SDA/I2S3_MCLK/EPHY0_25/PH_EINT13
PH14/I2S3_BCLK/RGMII0_RXD3/RMII0_NULL/PH_EINT14
PH15/I2S3_LRCK/RGMII0_RXD2/RMII0_NULL/PH_EINT15
PH16/I2S3_DOUT0/I2S3_DIN1/RGMII0_RXCK/RMII0_NULL/PH_EINT16
PH17/I2S3_DOUT1/I2S3_DIN0/RGMII0_TXD3/RMII0_NULL/PH_EINT17
PH18/CIR_OUT/I2S3_DOUT2/I2S3_DIN2/RGMII0_TXD2/RMII0_NULL/PH_EINT18
PH19/CIR_IN/I2S3_DOUT3/I2S3_DIN3/LEDC/PH_EINT19
PL0/S_TWI0_SCK/S_PL_EINT0
PL1/S_TWI0_SDA/S_PL_EINT1
PL2/S_UART_TX/S_PL_EINT2
PL3/S_UART_RX/S_PL_EINT3
PL4/S_JTAG_MS/S_PL_EINT4
PL5/S_JTAG_CK/S_PL_EINT5
PL6/S_JTAG_DO/S_PL_EINT6
PL7/S_JTAG_DI/S_PL_EINT7
PL8/S_TWI1_SCK/S_PL_EINT8
PL9/S_TWI1_SDA/S_PL_EINT9
PL10/S_PWM/S_PL_EINT10
PL11/S_CPU_CUR_W/S_CIR_IN/S_PL_EINT11
VCC_PL
A100-BGA-191130
NOTE:
Serial port data signal needs to be reversed.
Hardware ID
GPIO use gide:
1.Note that the voltage of SOC GPIO must matches the external IO voltage.
2.The pull up voltage of the GPIO is selected to correspond to the power field voltage of GPIO.
VCC-PC
VCC-PD
VCC-LVDS
VCC-PE
VCC-PL
VCC-PG
C38 100nF C0201
C39 100nF C0201
C40 100nF C0201
C41 100nF C0201
C42 100nF C0201
C43 100nF C0201
GND
AllWinner Technology Co.,Ltd
Design Name
A100_B3_AXP707_LPDDR3
Size A3
Page Name
07 SOC-GPIO
Rev
Date: Saturday, June 27, 2020
Sheet 7 of 18

LPDDR3



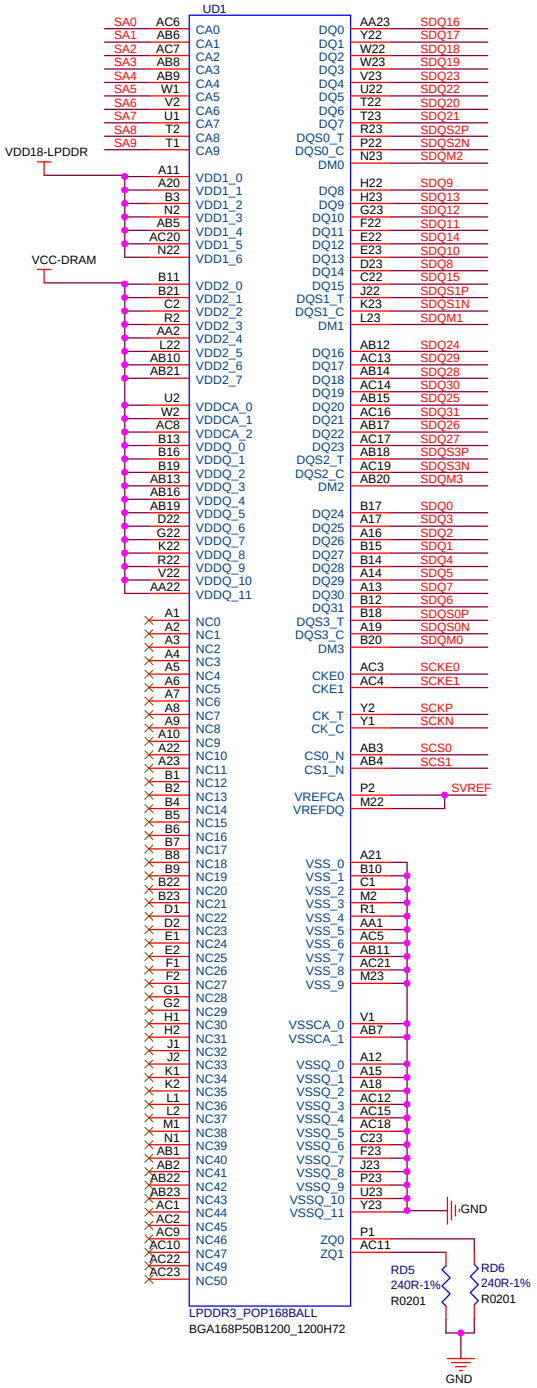


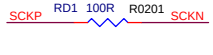


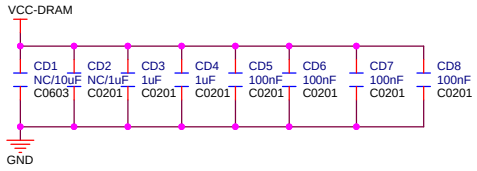
NOTE:

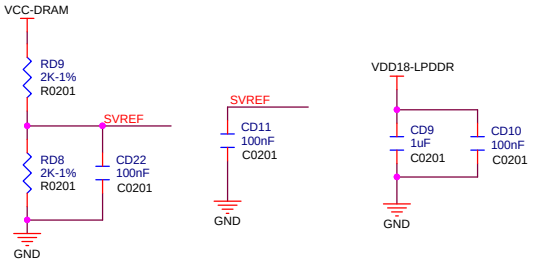
If use DDR3 4X4 model,due to the bandwidth of DDR,the system specification is limited as follows:

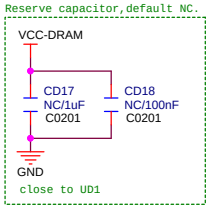
1. Max LCD resolution:<=1024*600@60Hz;
2. Not support 4K video encode and decode;
3. Not support miracase function.











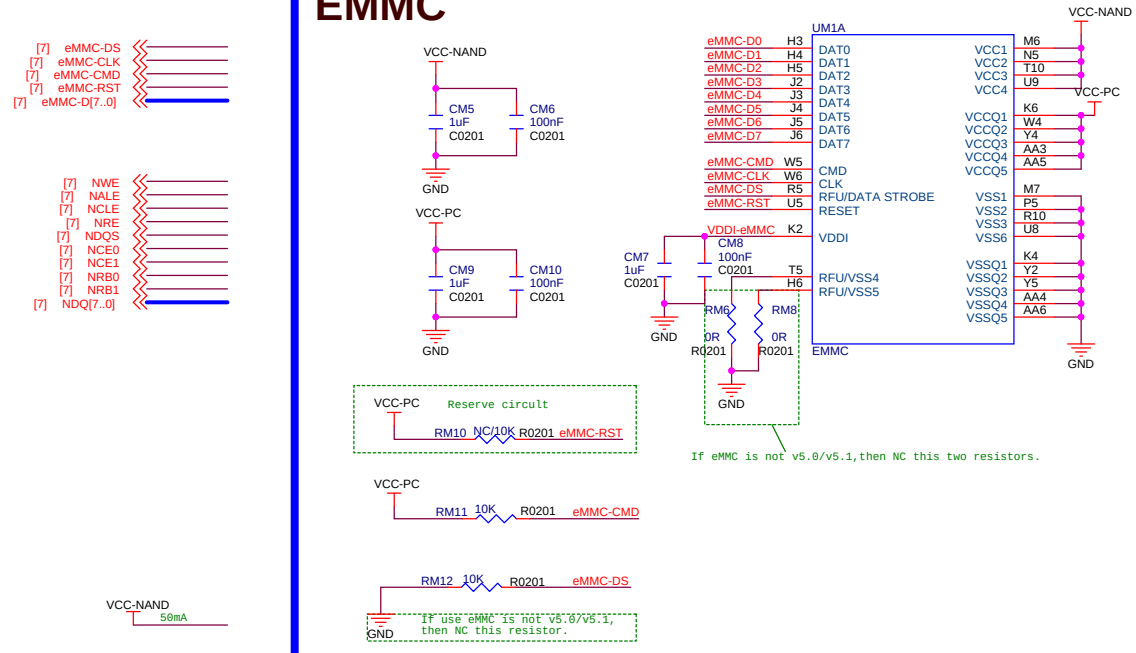
AllWinner Technology Co.,Ltd

Design Name: A100_B3_AXP707_LPDDR3

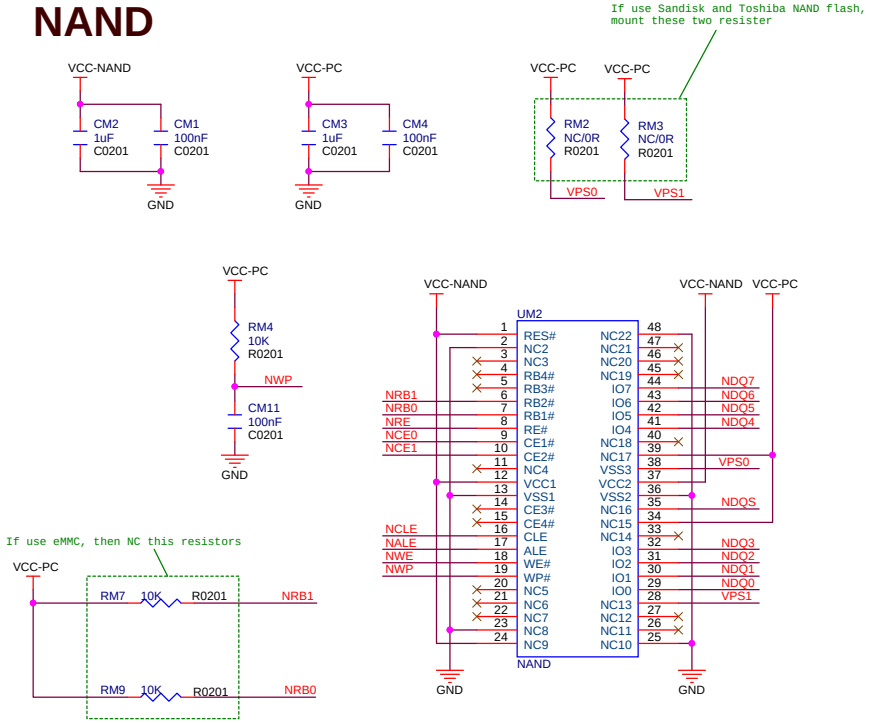
Size: A3 | Page Name: 08 LDDR3 | Rev:

Date: Friday, June 26, 2020 | Sheet 8 of 18

EMMC

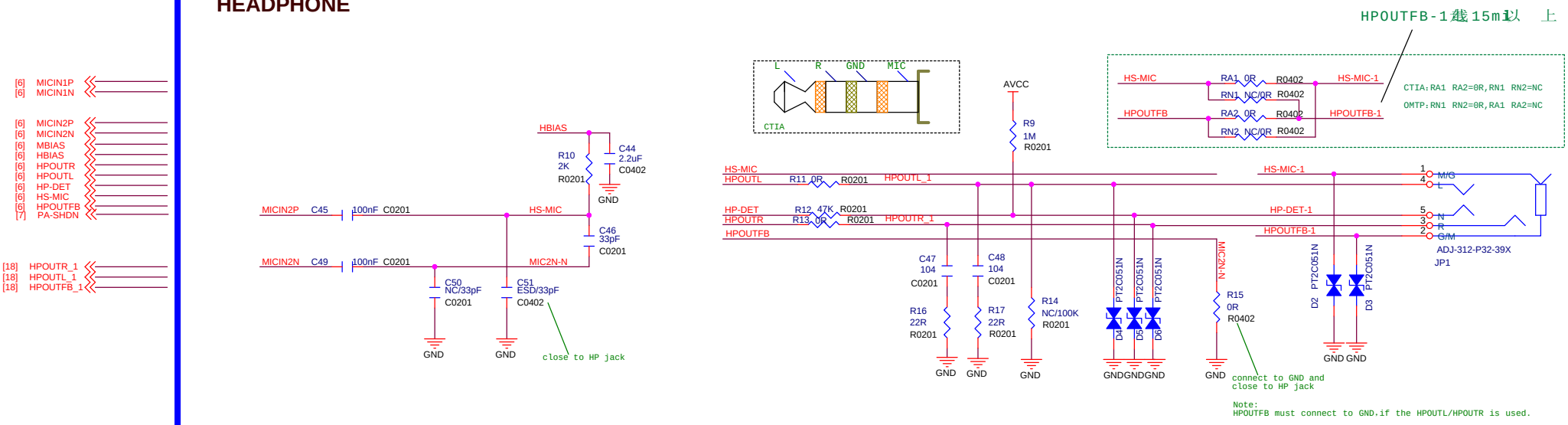


NAND



AllWinner Technology Co.,Ltd		
Design Name: A100_B3_AXP707_LPDDR3		
Size: A3	Page Name: 09 NAND/EMMC	Rev
Date: Saturday, April 25, 2020	Sheet 9 of 18	

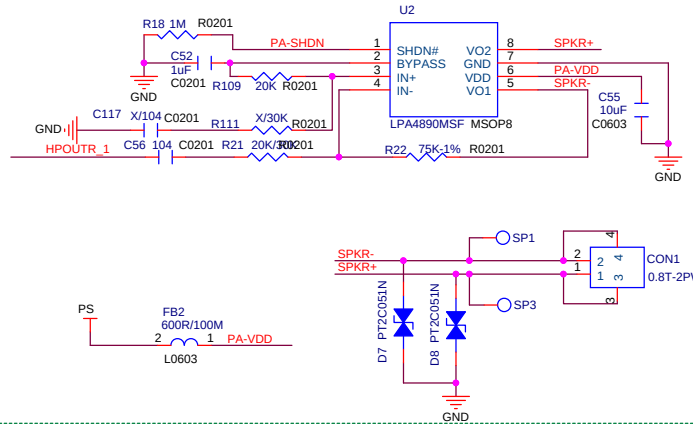
HEADPHONE

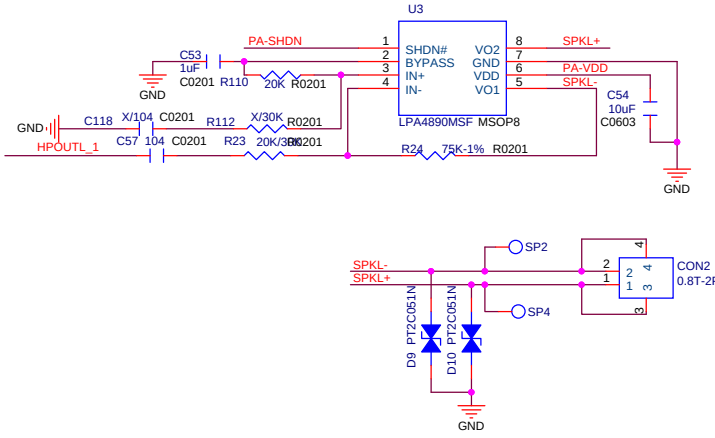


[6] MICIN1P
[6] MICIN1N
[6] MICIN2P
[6] MICIN2N
[6] MBIAS
[6] HBIAS
[6] HPOUTR
[6] HPOUTL
[6] HP-DET
[6] HS-MIC
[6] HPOUTFB
[7] PA-SHDN
[18] HPOUTR_1
[18] HPOUTL_1
[18] HPOUTFB_1

SPEAKER

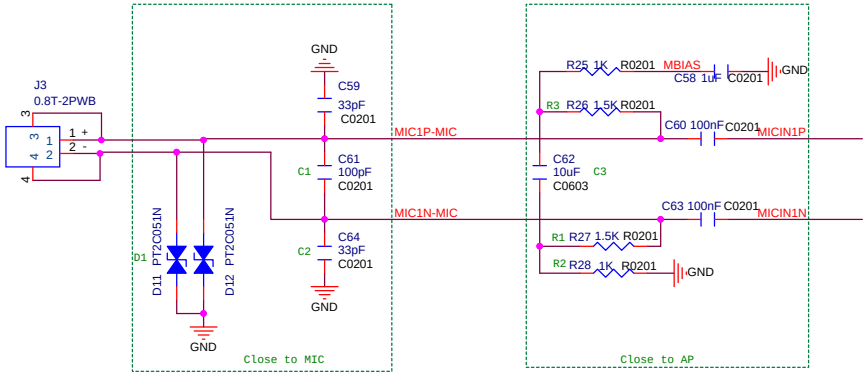
Default:R-OUT,SINGLE,SPEAKER





VCC-5V 1A
AVCC 15mA

MIC



Component	Diferential	single-ended
R1 R2 C1 C3 D1	USE	NC
C2	33pF	0R
R3	1.5K	1K

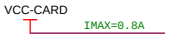
AllWinner Technology Co.,Ltd

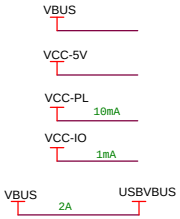
Design Name: A100_B3_AXP707_LPDDR3

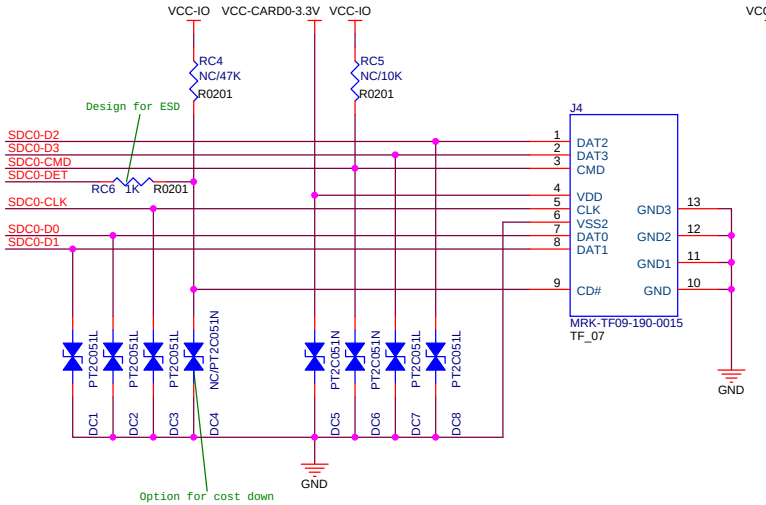
Size: A3 | Page Name: 10 AUDIO | Rev:

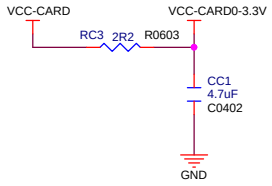
Date: Monday, April 27, 2020 | Sheet 10 of 18

SD CARD

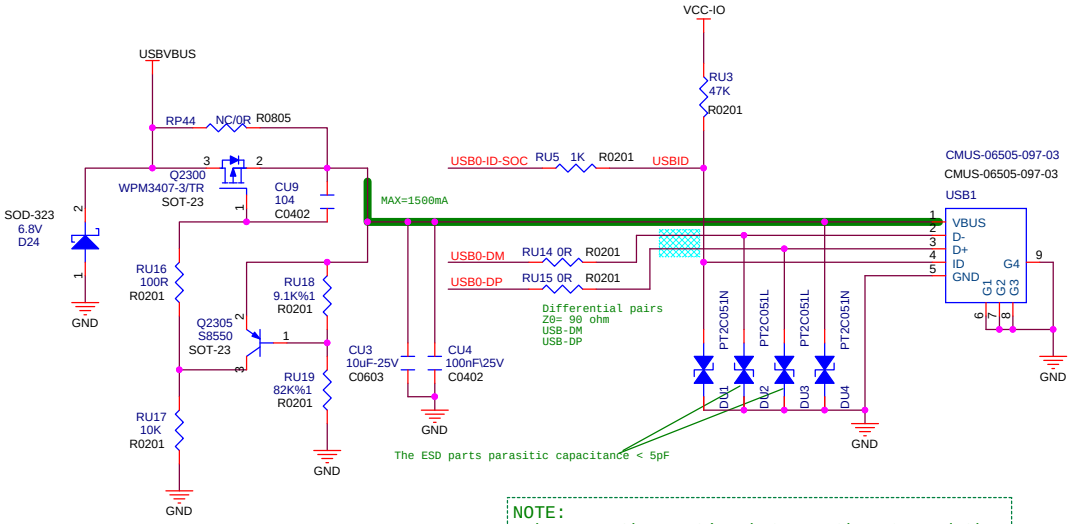








USB



NOTE:
Make sure the routing between the ESD and the USB connectors should be on the same PCB side

AllWinner Technology Co.,Ltd		
Design Name: A100_B3_AXP707_LPDDR3		
Size: A3	Page Name: 11 USB/CARD	Rev
Date: Saturday, July 04, 2020	Sheet 11 of 18	

MCSIA-D0[P/N]
MCSIA-D1[P/N]
MCSIA-D2[P/N]
MCSIA-D3[P/N]
MCSIA-CLK[P/N]
Differential pairs
Z0= 100 ohm

MCSIB-D0[P/N]
MCSIB-D1[P/N]
MCSIB-CLK[P/N]
Differential pairs
Z0= 100 ohm

[6] MCSIA-CLKN
[6] MCSIA-CLKP
[6] MCSIA-D3N
[6] MCSIA-D3P
[6] MCSIA-D2N
[6] MCSIA-D2P
[6] MCSIA-D1N
[6] MCSIA-D1P
[6] MCSIA-D0N
[6] MCSIA-D0P
[6] MCSIB-CLKN
[6] MCSIB-CLKP
[6] MCSIB-D0N
[6] MCSIB-D0P
[6] MCSIB-D1N
[6] MCSIB-D1P
[7] MCSI-MCLK
[7] MCSI-SCK
[7] MCSI-SDA
[7] MCSI-STBY-F
[7] MCSI-RST-F
[7] MCSI-STBY-R
[7] MCSI-RST-R
[7] LED-EN

VCC-PE
R29 100K R0201 MCSI-RST-F
R30 100K R0201 MCSI-STBY-F
VCC-PE
R94 100K R0201 MCSI-RST-R
R31 100K R0201 MCSI-STBY-R

AFVCC-CSI AVDD-CSI IOVDD-CSI DVDD-CSI
C103 1uF C0201
C66 4.7uF C0402
C67 1uF C0201
C68 1uF C0201
GND GND GND GND

NOTE:
Close to connector
C65 NC C0201
GND

CON3
1 GND0
2 MDN3_B
3 MDP3_B
4 GND1
5 MDN2_B
6 MDP2_B
7 GND2
8 MCSIA-D1N
9 MCSIA-D1P
10 MDP1_B
11 GND3
12 MCSIA-D0N
13 MCSIA-D0P
14 MDP0_B
15 GND4
16 MCSIA-CLKN
17 MCSIA-CLKP
18 MCN_B
19 MCP_B
20 GND5
21 MDN1_F
22 MDP1_F
23 GND6
24 MCSIB-D0N
25 MCSIB-D0P
26 MDN0_F
27 MDP0_F
28 GND7
29 MCSIB-CLKN
30 MCSIB-CLKP
31 MCN_F
32 MCP_F
33 GND8
34 MCSI-MCLK
35 FLASH_LED+
36 MCLK_F
37 GND9
38 MCSI-MCLK
39 FLASH_LED-
40 MCLK_B
41 GND10
PWDN_F
RESET_F
RESET_B
PWDN_B
SCL
SDA
AF_VDD28
DVDD
AVDD28
DOVDD18
40
41
CON39PIN
GND
AFVCC-CSI
DVDD-CSI
AVDD-CSI
IOVDD-CSI

NOTE:

1.The working voltage and current of power need determine according to the peripheral specification.

2.AFVCC-CSI has timing requirements, don't share the same power with DOVDD-CSI.

3.The front and rear cameras need to consider the compatibility of DVDD-CSI voltage.

VCC-PE
R32 2K R0201 MCSI-SDA
R33 2K R0201 MCSI-SCK

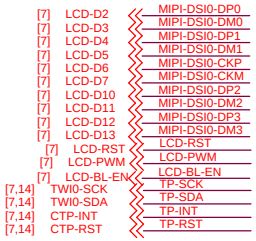
VBAT 100mA
VCC-PL 10mA
AVDD-CSI 2.8V@30mA
IOVDD-CSI 1.8V@20mA
DVDD-CSI 1.2V@25mA
VCC-PE 10mA
AFVCC-CSI 2.8V@100mA

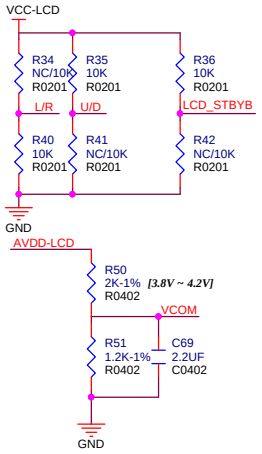
FLASH_LED

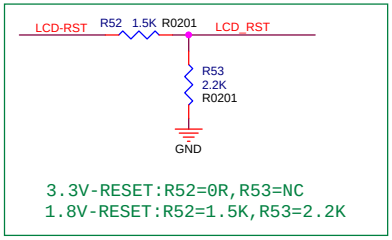
VCC-5V
FR1 100R R0603
FLASH_LED+
PAD2PIN
2
FC1 104 C0201
FLASH_LED-
1
J6
GND
LED-EN
FR2 10K R0201
3
1
FQ1 SOT-23 MMBT3904
2
FR4 100K R0201
FC2 104 C0201
GND GND GND

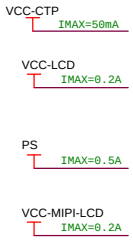
AllWinner Technology Co.,Ltd		
Design Name: A100_B3_AXP707_LPDDR3		
Size: A3	Page Name: 12 CAMERA	Rev
Date: Monday, April 27, 2020	Sheet 12 of 18	

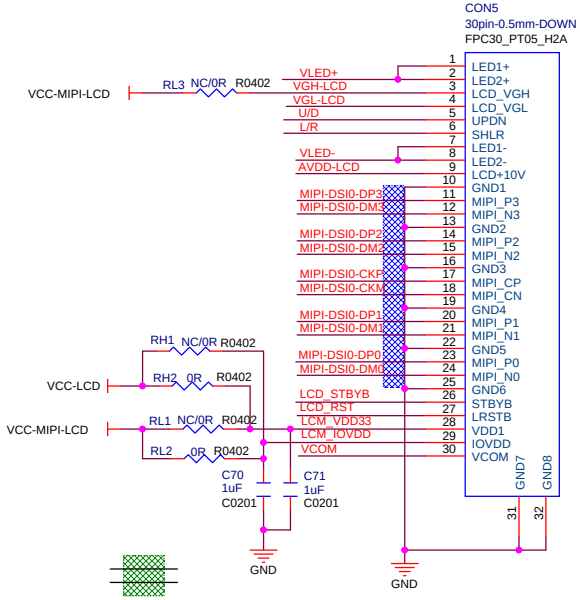
LCD



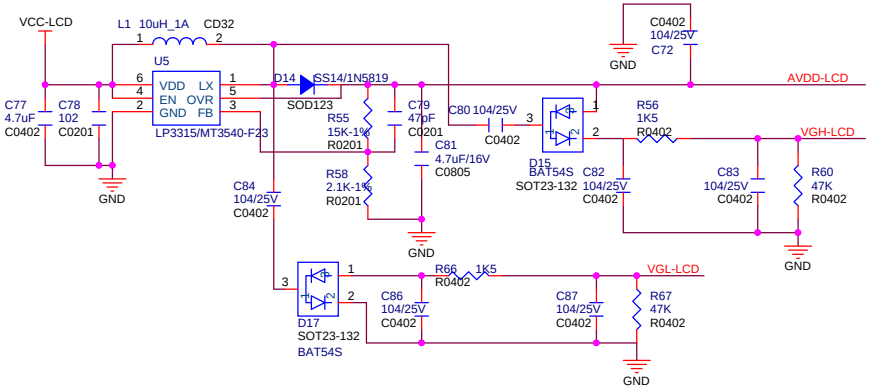




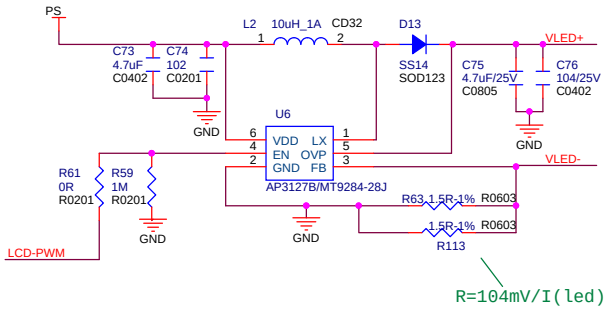




LCD POWER

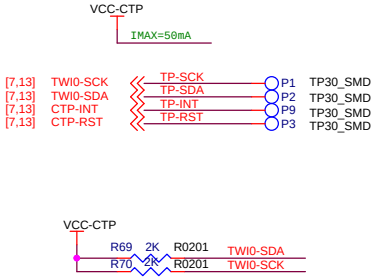


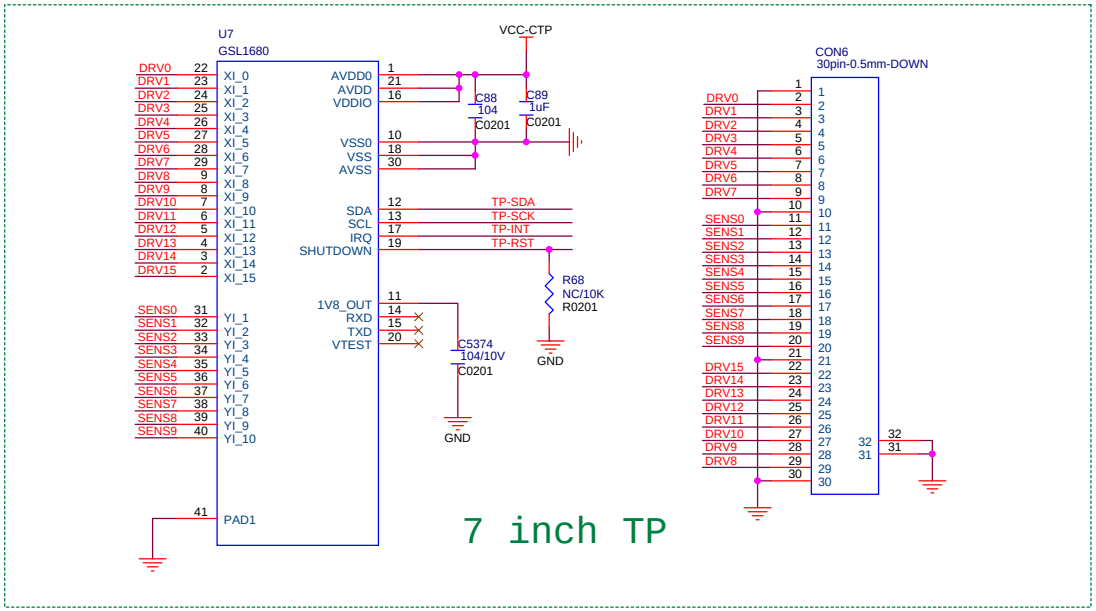
BACKLIGHT

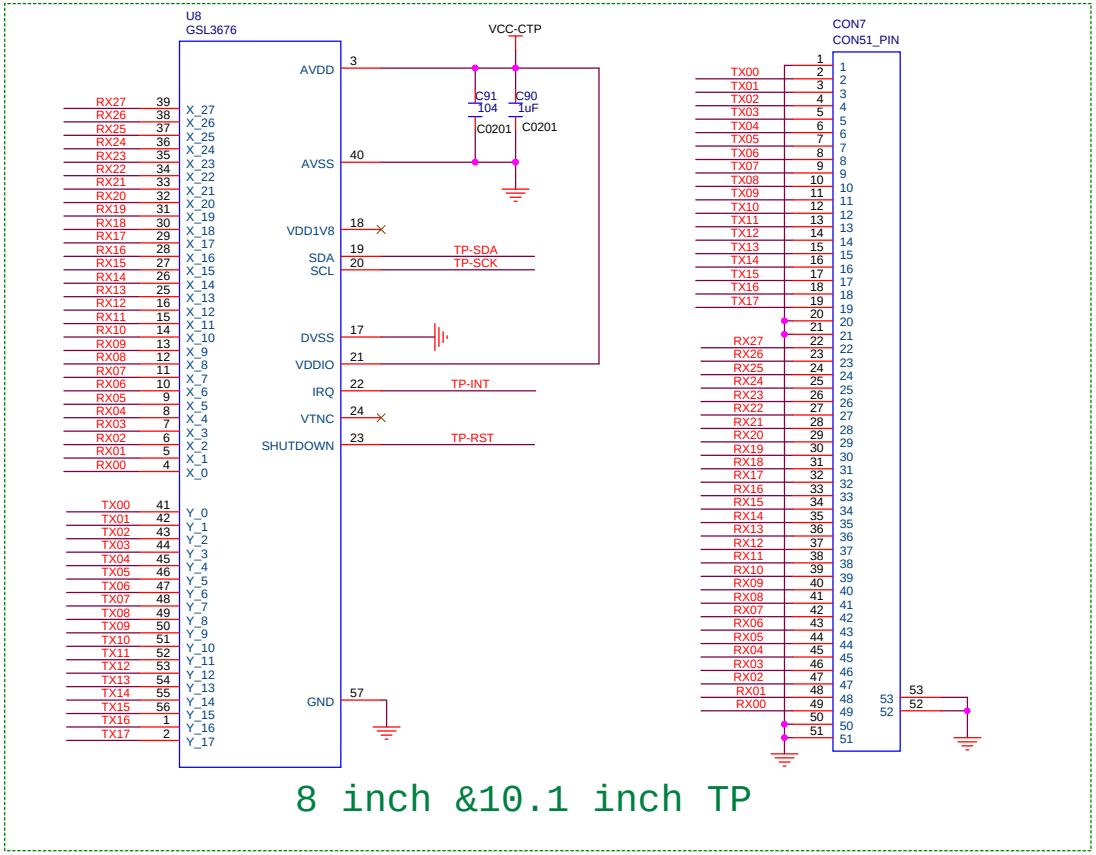


AllWinner Technology Co.,Ltd		
Design Name: A100_B3_AXP707_LPDDR3		
Size: A3	Page Name: 13 LCM	Rev
Date: Monday, June 08, 2020	Sheet 13 of 18	

CTP

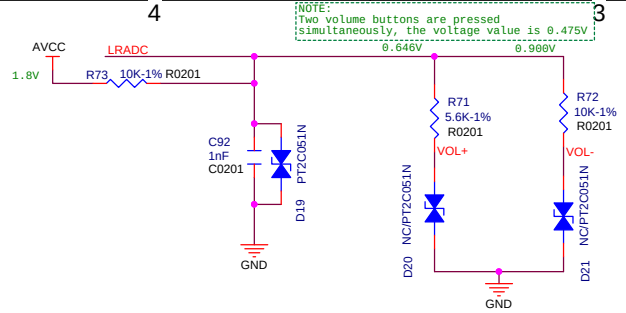




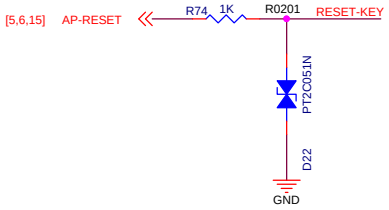


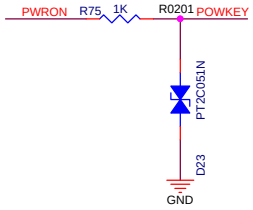
AllWinner Technology Co.,Ltd	
Design Name	A100_B3_AXP707_LPDDR3
Size A3 / Page Name	14 CTP
Rev	
Date: Wednesday, April 29, 2020	Sheet 14 of 18

KEY

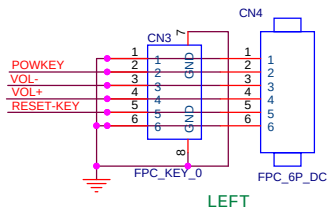


RIGHT





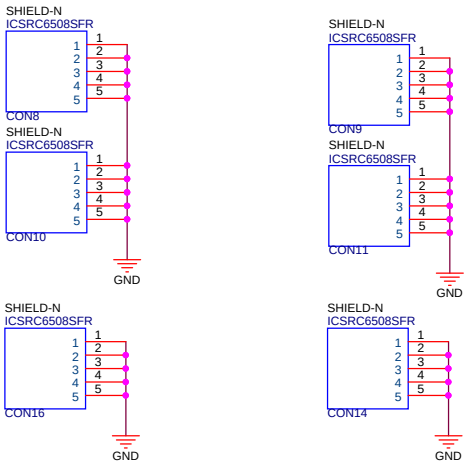
NOTE:
Put the testpoint together
Mark Signal Name On PCB Silkscreen



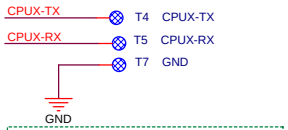
LEFT

SHIELD

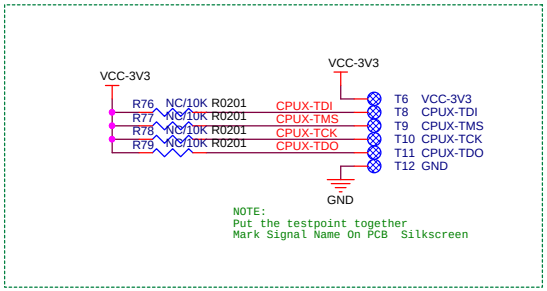
SOC&DDR&PMU mask clamp



CPUX DEBUG

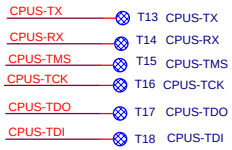


NOTE:
Put the testpoint together
Mark Signal Name On PCB Silkscreen

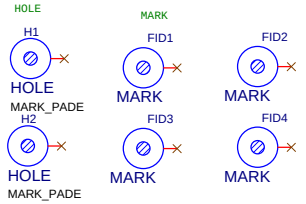


NOTE:
Put the testpoint together
Mark Signal Name On PCB Silkscreen

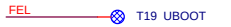
CPUS DEBUG



ASSEMBLE



FEL

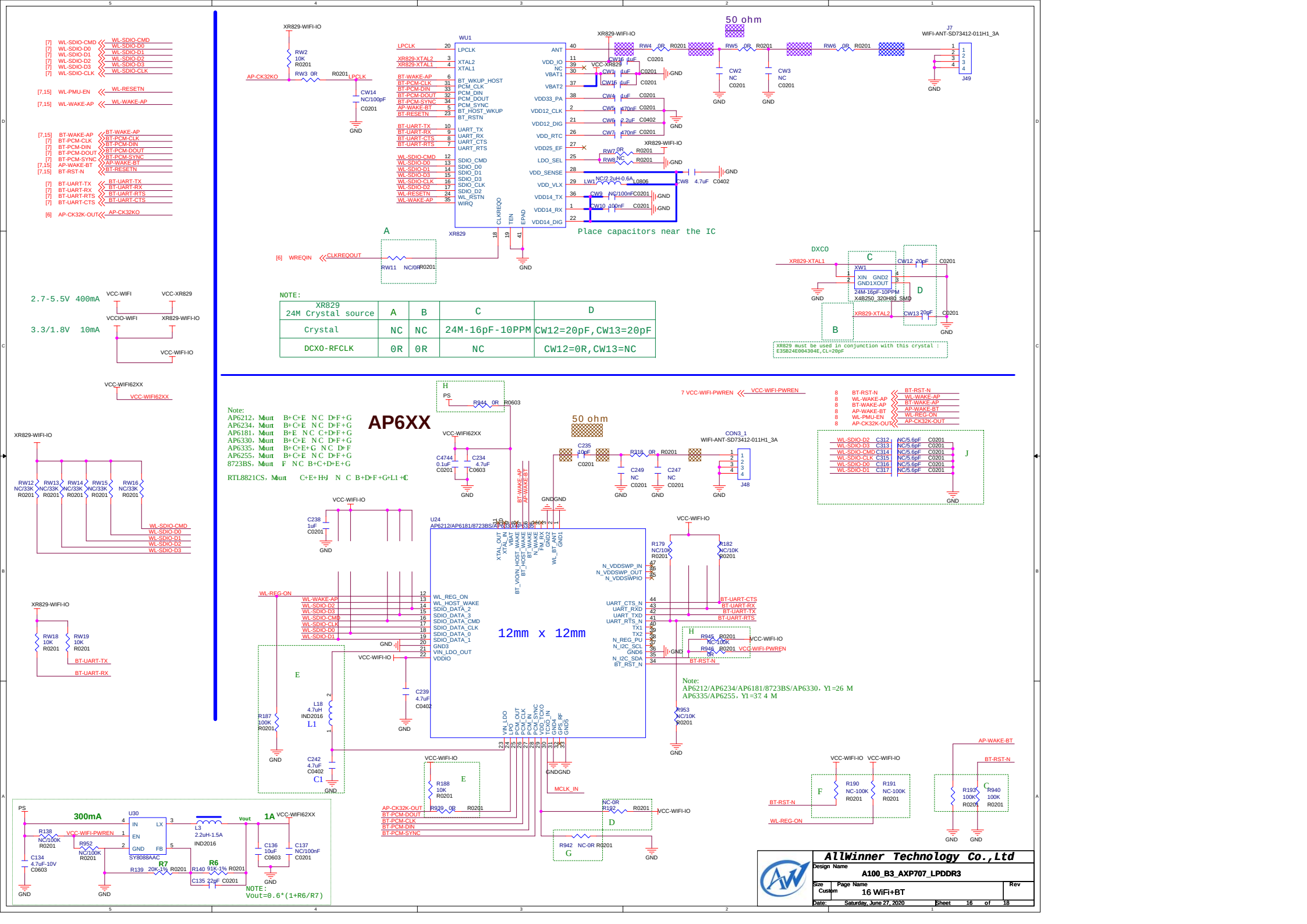


[5,6,15] AP-RESET
[6] LRADC
[5] PWRON
[6] FEL
AVCC 1mA
VCC-3V3 20mA

[7] CPUX-TX
[7] CPUX-RX
[7,18] CPUX-TDI
[7] CPUX-TMS
[7] CPUX-TCK
[7] CPUX-TDO

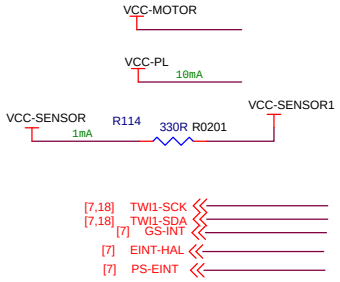
[7,16] CPUS-TX
[7,16] CPUS-RX
[7,16] CPUS-TMS
[7,16] CPUS-TCK
[7,16] CPUS-TDO
[7] CPUS-TDI

AllWinner Technology Co.,Ltd			
Design Name	A100_B3_AXP707_LPDDR3		
Size A3	Page Name 15 KEY/DEBUG		Rev
Date: Monday, April 27, 2020	Sheet 15 of 18		

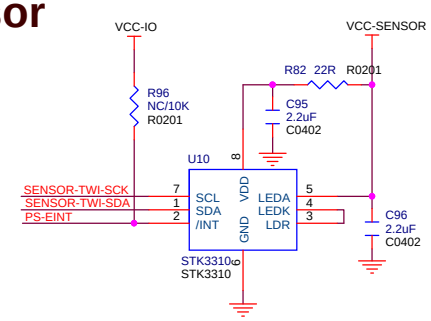


Design Name	A100_B3_AXP707_LPDDR3
Size / Custom	
Page Name	16 WiFi+BT
Rev	
Date:	Saturday, June 27, 2020
Sheet	16 of 18

AllWinner Technology Co.,Ltd

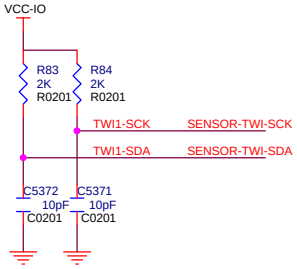


ALS Sensor



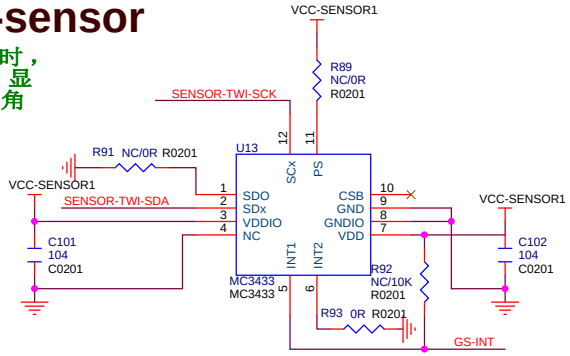
I2C Address: 0x48

ALS Sensor CON

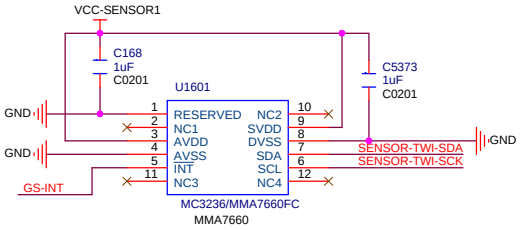


3axis G-sensor

正视显示屏时，第一 PIN朝向显示屏的左上角



I2C Address: 0x19



Hall switch

Motor

AllWinner Technology Co.,Ltd		
Design Name: A100_B3_AXP707_LPDDR3		
Size: A3	Page Name: 17 SENSOR	Rev
Date: Monday, April 27, 2020	Sheet 17 of 18	