APOLLO LAKE

Y116AR100

LPDDR3 216 Ball x2

APOLLO LAKE		
Title: APOLLO LAKE		
Size: Custom	Document Number: COVER PAGE	Rev: R100
Date: Tuesday, December 06, 2016	Sheet 1 of 57	

TABLE OF CONTENTS

SHEET NO.	SHEET NAME
1	COVER PAGE
2	TABLE OF CONTENTS
3	APOLLO LAKE SOC (DDR CH A)
4	APOLLO LAKE SOC (DDR CH B)
5	APOLLO LAKE SOC (USB,PCIE,SATA)
6	APOLLO LAKE SOC (DDI)
7	APOLLO LAKE SOC (CSI-MIPI, EMMC,I2C,SPI)
8	APOLLO LAKE SOC(PMU)
9	APOLLO LAKE SOC (POWER)
10	APOLLO LAKE SOC (GND)
11	NC
12	NC
13	NC
14	NC
15	NC
16	NC
17	APOLLO LAKE SOC (DECOUPLING)
18	APOLLO LAKE SOC (BOOTSTRAP)
19	LPDDR3 CH-A
20	LPDDR3 CH-B
21	LPDDR3 CH-A TERMINATIONS
22	LPDDR3 CH-B TERMINATIONS
23	LPDDR3 DECOUPLING
24	SYSTEM FLASH
25	EMMC
26	SATA SSD MODULE
27	MICRO-SD CARD
28	SDCARD POWER
29	POWER DELIVERY 5V/3.3V
30	PMIC1
31	PMIC2
32	PMIC3
33	PMIC4
34	HDMI LEVEL SHIFTERS
35	HDMI CONNECTOR
36	DISPLAY
37	FINGER PRINT
38	SENSORS
39	NC
40	NC

SHEET NO.	SHEET NAME
41	NC
42	USB3.0 CONN
43	WLAN WIFI BT MODULE
44	HDD CONN
45	SIM CONN
46	AUDIO CODEC
47	SPK&IO CONN
48	BATTERY CHARGER
49	NC
50	EMBEDDED CONTROLLER
51	BUTTONS LEDS AND MISC
52	NC
53	DC-IN
54	NC
55	NC
56	DEBUG
57	FACTORY TEST POINTS

I2C TABLE

INTERFACE	ISH-I2C0	ISH-I2C1	ISH-I2C2	I2C-0	I2C-1	I2C-2	I2C-3	I2C-4
TOUCH CONTROLLER					0X10			
ACCELROMETER	0X18							
GYRO	0X68							
ALS	0X10							
SAR PROX	0X28							
FRONT CAMERA						0X10		
REAR CAMERA SENSOR						0X36		
REAR CAMERA VCM						0X0C		
WWAN-GNSS			TBD					
Wireless Charging				TBD				

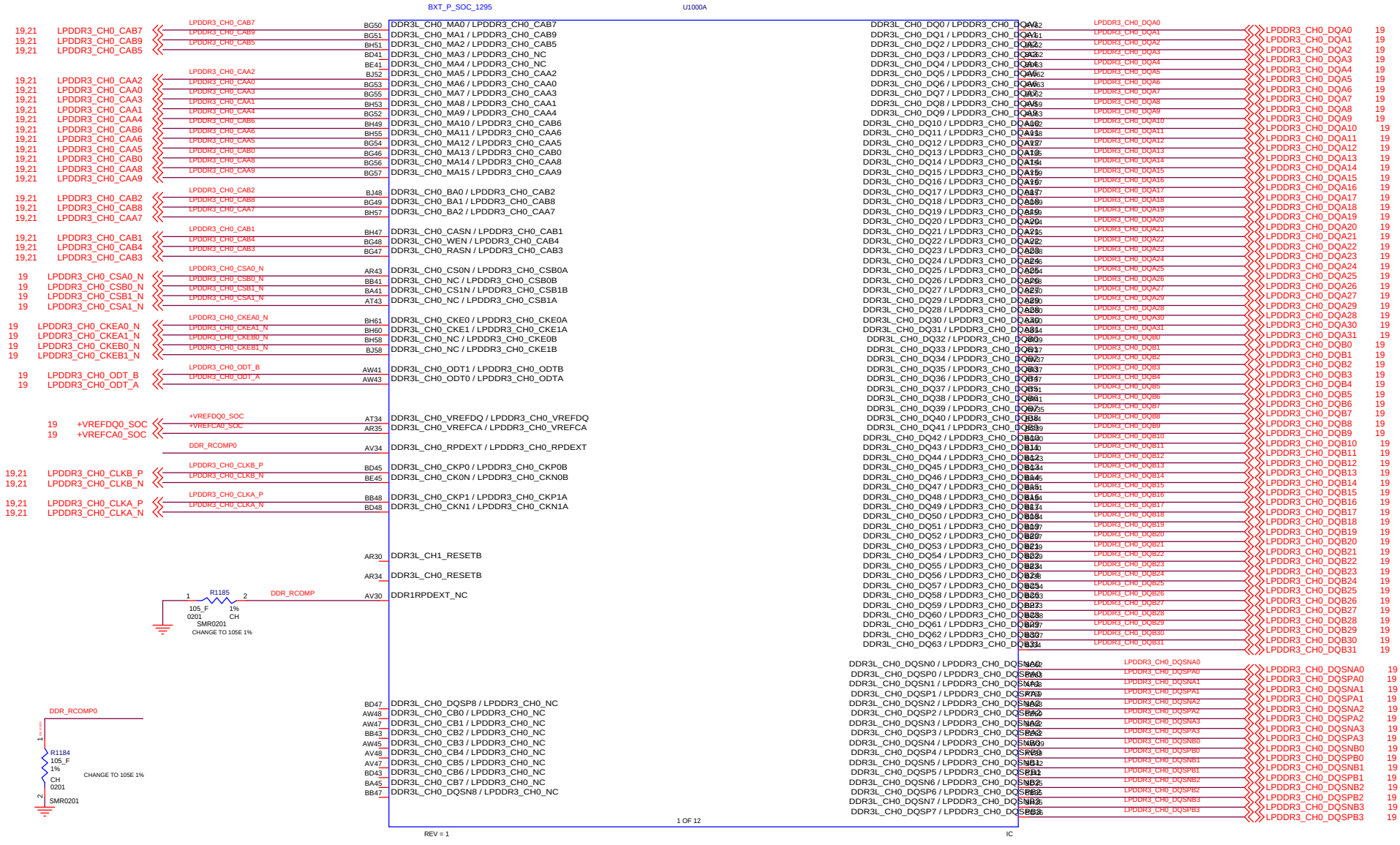
EC I2C INTERFACE	EC_12C-0
TYPE-C PD CONTROLLER	0XC0
BATTERY CHARGER	TBD
EEPROM	0XA0

APOLLO LAKE

Title: APOLLO LAKE

Size: Custom | Document Number: TABLE OF CONTENTS | Rev: R100

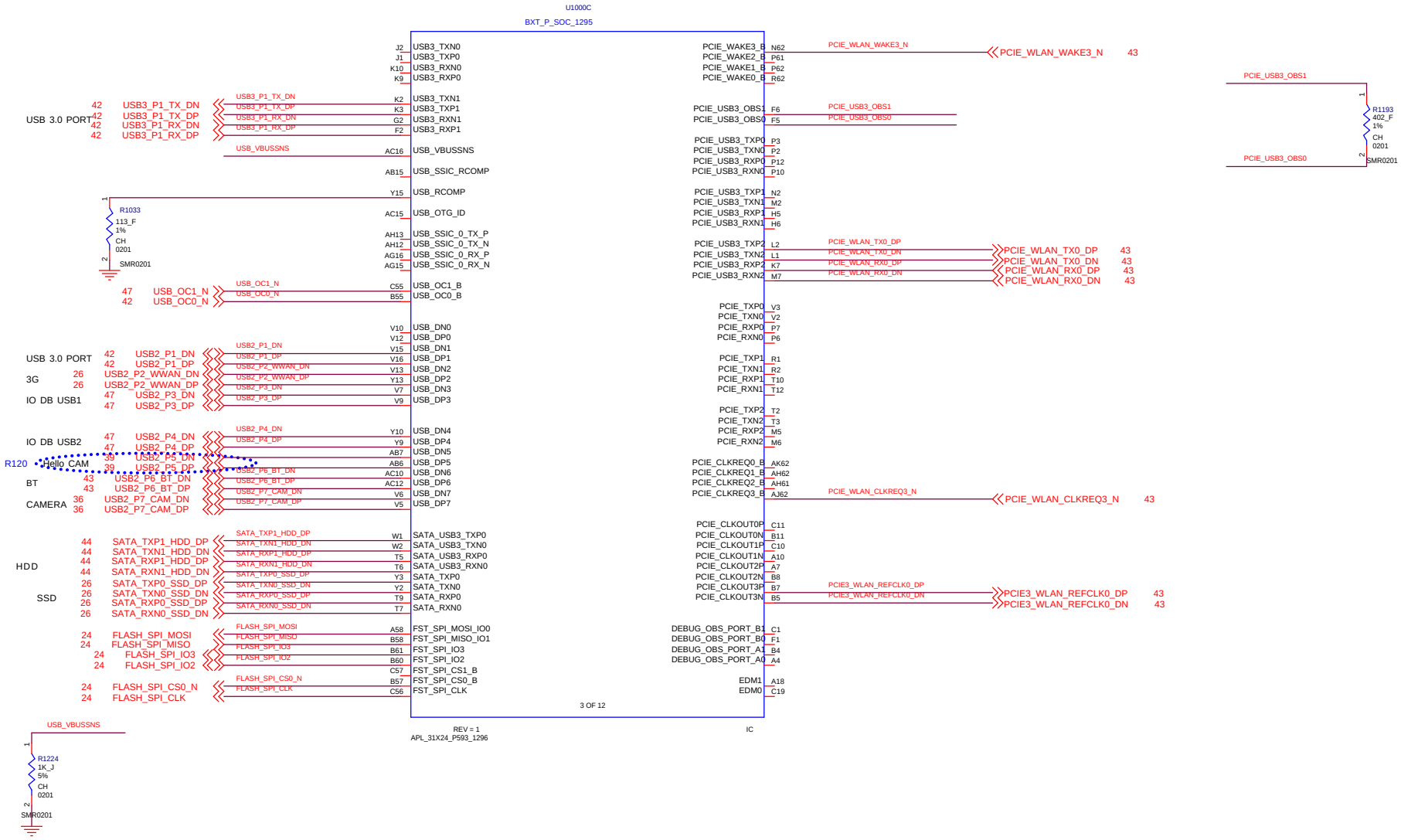
Date: Tuesday, December 06, 2016 | Sheet 2 of 57



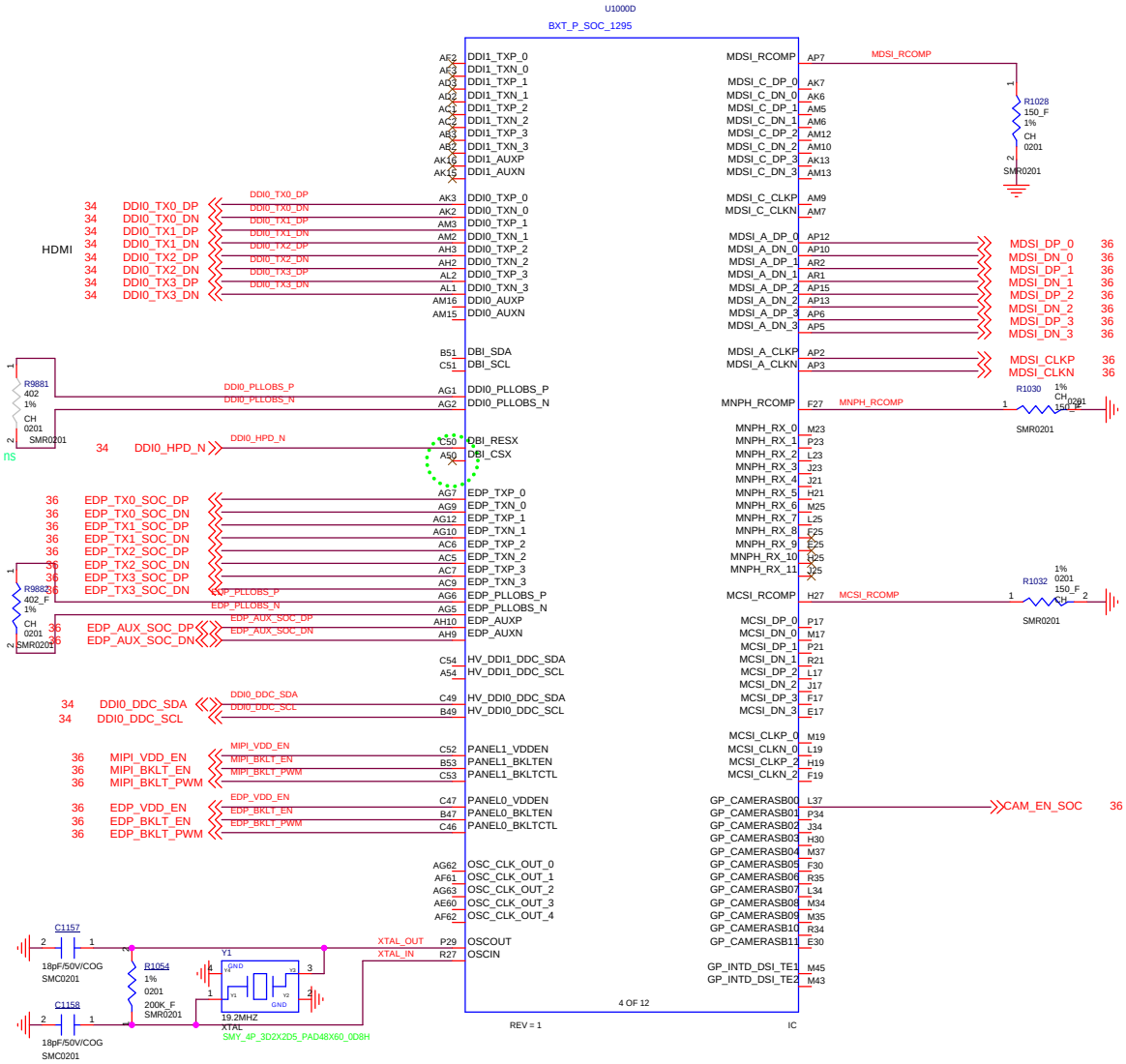
Title	APOLLO LAKE
Size	Custom
Document Number	LPDDR3-CPU
Rev	R100
Date:	Tuesday, December 06, 2016
Sheet	3 of 57

20,22	LPDDR3_CH1_CAB7	LPDDR3_CH1_CAB7	BG9	DDR3L_CH1_DQ0 / LPDDR3_CH1_DQA0	BJ26	LPDDR3_CH1_DQA0	LPDDR3_CH1_DQA0 20
20,22	LPDDR3_CH1_CAB9	LPDDR3_CH1_CAB9	BG10	DDR3L_CH1_DQ1 / LPDDR3_CH1_DQA1	BG30	LPDDR3_CH1_DQA1	LPDDR3_CH1_DQA1 20
20,22	LPDDR3_CH1_CAB5	LPDDR3_CH1_CAB5	BH9	DDR3L_CH1_DQ2 / LPDDR3_CH1_DQA2	BH31	LPDDR3_CH1_DQA2	LPDDR3_CH1_DQA2 20
			BD16	DDR3L_CH1_DQ3 / LPDDR3_CH1_DQA3	BG31	LPDDR3_CH1_DQA3	LPDDR3_CH1_DQA3 20
			BB16	DDR3L_CH1_DQ4 / LPDDR3_CH1_DQA4	BH27	LPDDR3_CH1_DQA4	LPDDR3_CH1_DQA4 20
20,22	LPDDR3_CH1_CAA2	LPDDR3_CH1_CAA2	BG11	DDR3L_CH1_DQ5 / LPDDR3_CH1_DQA5	BG27	LPDDR3_CH1_DQA5	LPDDR3_CH1_DQA5 20
20,22	LPDDR3_CH1_CAA0	LPDDR3_CH1_CAA0	BJ12	DDR3L_CH1_DQ6 / LPDDR3_CH1_DQA6	BG26	LPDDR3_CH1_DQA6	LPDDR3_CH1_DQA6 20
20,22	LPDDR3_CH1_CAA3	LPDDR3_CH1_CAA3	BG14	DDR3L_CH1_DQ7 / LPDDR3_CH1_DQA7	BJ30	LPDDR3_CH1_DQA7	LPDDR3_CH1_DQA7 20
20,22	LPDDR3_CH1_CAA1	LPDDR3_CH1_CAA1	BG12	DDR3L_CH1_DQ8 / LPDDR3_CH1_DQA8	BA30	LPDDR3_CH1_DQA8	LPDDR3_CH1_DQA8 20
20,22	LPDDR3_CH1_CAA4	LPDDR3_CH1_CAA4	BH11	DDR3L_CH1_DQ9 / LPDDR3_CH1_DQA9	BB30	LPDDR3_CH1_DQA9	LPDDR3_CH1_DQA9 20
20,22	LPDDR3_CH1_CAB6	LPDDR3_CH1_CAB6	BG7	DDR3L_CH1_DQ10 / LPDDR3_CH1_DQA10	BE30	LPDDR3_CH1_DQA10	LPDDR3_CH1_DQA10 20
20,22	LPDDR3_CH1_CAA6	LPDDR3_CH1_CAA6	BH13	DDR3L_CH1_DQ11 / LPDDR3_CH1_DQA11	BD30	LPDDR3_CH1_DQA11	LPDDR3_CH1_DQA11 20
20,22	LPDDR3_CH1_CAA5	LPDDR3_CH1_CAA5	BG13	DDR3L_CH1_DQ12 / LPDDR3_CH1_DQA12	BE25	LPDDR3_CH1_DQA12	LPDDR3_CH1_DQA12 20
20,22	LPDDR3_CH1_CAB0	LPDDR3_CH1_CAB0	BH3	DDR3L_CH1_DQ13 / LPDDR3_CH1_DQA13	BB27	LPDDR3_CH1_DQA13	LPDDR3_CH1_DQA13 20
20,22	LPDDR3_CH1_CAA8	LPDDR3_CH1_CAA8	BG15	DDR3L_CH1_DQ14 / LPDDR3_CH1_DQA14	BD25	LPDDR3_CH1_DQA14	LPDDR3_CH1_DQA14 20
20,22	LPDDR3_CH1_CAA9	LPDDR3_CH1_CAA9	BG16	DDR3L_CH1_DQ15 / LPDDR3_CH1_DQA15	BD27	LPDDR3_CH1_DQA15	LPDDR3_CH1_DQA15 20
				DDR3L_CH1_DQ16 / LPDDR3_CH1_DQA16	BG24	LPDDR3_CH1_DQA16	LPDDR3_CH1_DQA16 20
20,22	LPDDR3_CH1_CAB2	LPDDR3_CH1_CAB2	BH6	DDR3L_CH1_DQ17 / LPDDR3_CH1_DQA17	BJ20	LPDDR3_CH1_DQA17	LPDDR3_CH1_DQA17 20
20,22	LPDDR3_CH1_CAB8	LPDDR3_CH1_CAB8	BG8	DDR3L_CH1_DQ18 / LPDDR3_CH1_DQA18	BH23	LPDDR3_CH1_DQA18	LPDDR3_CH1_DQA18 20
20,22	LPDDR3_CH1_CAA7	LPDDR3_CH1_CAA7	BH15	DDR3L_CH1_DQ19 / LPDDR3_CH1_DQA19	BJ24	LPDDR3_CH1_DQA19	LPDDR3_CH1_DQA19 20
				DDR3L_CH1_DQ20 / LPDDR3_CH1_DQA20	BG20	LPDDR3_CH1_DQA20	LPDDR3_CH1_DQA20 20
20,22	LPDDR3_CH1_CAB3	LPDDR3_CH1_CAB3	BJ6	DDR3L_CH1_DQ21 / LPDDR3_CH1_DQA21	BG21	LPDDR3_CH1_DQA21	LPDDR3_CH1_DQA21 20
20,22	LPDDR3_CH1_CAB1	LPDDR3_CH1_CAB1	BH4	DDR3L_CH1_DQ22 / LPDDR3_CH1_DQA22	BH19	LPDDR3_CH1_DQA22	LPDDR3_CH1_DQA22 20
20,22	LPDDR3_CH1_CAB4	LPDDR3_CH1_CAB4	BH7	DDR3L_CH1_DQ23 / LPDDR3_CH1_DQA23	BG25	LPDDR3_CH1_DQA23	LPDDR3_CH1_DQA23 20
				DDR3L_CH1_DQ24 / LPDDR3_CH1_DQA24	AT27	LPDDR3_CH1_DQA24	LPDDR3_CH1_DQA24 20
20	LPDDR3_CH1_CSB1_N	LPDDR3_CH1_CSB1_N	AW17	DDR3L_CH1_DQ25 / LPDDR3_CH1_DQA25	AW29	LPDDR3_CH1_DQA25	LPDDR3_CH1_DQA25 20
20	LPDDR3_CH1_CSB0_N	LPDDR3_CH1_CSB0_N	AV17	DDR3L_CH1_DQ26 / LPDDR3_CH1_DQA26	AR27	LPDDR3_CH1_DQA26	LPDDR3_CH1_DQA26 20
20	LPDDR3_CH1_CSA1_N	LPDDR3_CH1_CSA1_N	BB17	DDR3L_CH1_DQ27 / LPDDR3_CH1_DQA27	AT23	LPDDR3_CH1_DQA27	LPDDR3_CH1_DQA27 20
20	LPDDR3_CH1_CSA0_N	LPDDR3_CH1_CSA0_N	BD17	DDR3L_CH1_DQ28 / LPDDR3_CH1_DQA28	AV27	LPDDR3_CH1_DQA28	LPDDR3_CH1_DQA28 20
				DDR3L_CH1_DQ29 / LPDDR3_CH1_DQA29	AR25	LPDDR3_CH1_DQA29	LPDDR3_CH1_DQA29 20
20	LPDDR3_CH1_CKEA0_N	LPDDR3_CH1_CKEA0_N	BG18	DDR3L_CH1_DQ30 / LPDDR3_CH1_DQA30	AR23	LPDDR3_CH1_DQA30	LPDDR3_CH1_DQA30 20
20	LPDDR3_CH1_CKEA1_N	LPDDR3_CH1_CKEA1_N	BG17	DDR3L_CH1_DQ31 / LPDDR3_CH1_DQA31	AW27	LPDDR3_CH1_DQA31	LPDDR3_CH1_DQA31 20
20	LPDDR3_CH1_CKEB0_N	LPDDR3_CH1_CKEB0_N	BH17	DDR3L_CH1_DQ32 / LPDDR3_CH1_DQB0	BF6	LPDDR3_CH1_DQB0	LPDDR3_CH1_DQB0 20
20	LPDDR3_CH1_CKEB1_N	LPDDR3_CH1_CKEB1_N	BJ16	DDR3L_CH1_DQ33 / LPDDR3_CH1_DQB1	BD10	LPDDR3_CH1_DQB1	LPDDR3_CH1_DQB1 20
				DDR3L_CH1_DQ34 / LPDDR3_CH1_DQB2	BE14	LPDDR3_CH1_DQB2	LPDDR3_CH1_DQB2 20
20	LPDDR3_CH1_ODT_A	LPDDR3_CH1_ODT_A	AW16	DDR3L_CH1_DQ35 / LPDDR3_CH1_DQB3	BB10	LPDDR3_CH1_DQB3	LPDDR3_CH1_DQB3 20
20	LPDDR3_CH1_ODT_B	LPDDR3_CH1_ODT_B	AV16	DDR3L_CH1_DQ36 / LPDDR3_CH1_DQB4	BA14	LPDDR3_CH1_DQB4	LPDDR3_CH1_DQB4 20
				DDR3L_CH1_DQ37 / LPDDR3_CH1_DQB5	BB14	LPDDR3_CH1_DQB5	LPDDR3_CH1_DQB5 20
				DDR3L_CH1_DQ38 / LPDDR3_CH1_DQB6	BD14	LPDDR3_CH1_DQB6	LPDDR3_CH1_DQB6 20
				DDR3L_CH1_DQ39 / LPDDR3_CH1_DQB7	BE8	LPDDR3_CH1_DQB7	LPDDR3_CH1_DQB7 20
20	+VREFDQ1_SOC	+VREFDQ1_SOC	AT30	DDR3L_CH1_DQ40 / LPDDR3_CH1_DQB8	AV12	LPDDR3_CH1_DQB8	LPDDR3_CH1_DQB8 20
20	+VREFCA1_SOC	+VREFCA1_SOC	AR29	DDR3L_CH1_DQ41 / LPDDR3_CH1_DQB9	BD6	LPDDR3_CH1_DQB9	LPDDR3_CH1_DQB9 20
				DDR3L_CH1_DQ42 / LPDDR3_CH1_DQB10	BD5	LPDDR3_CH1_DQB10	LPDDR3_CH1_DQB10 20
				DDR3L_CH1_DQ43 / LPDDR3_CH1_DQB11	BB7	LPDDR3_CH1_DQB11	LPDDR3_CH1_DQB11 20
				DDR3L_CH1_DQ44 / LPDDR3_CH1_DQB12	AV10	LPDDR3_CH1_DQB12	LPDDR3_CH1_DQB12 20
				DDR3L_CH1_DQ45 / LPDDR3_CH1_DQB13	AY9	LPDDR3_CH1_DQB13	LPDDR3_CH1_DQB13 20
				DDR3L_CH1_DQ46 / LPDDR3_CH1_DQB14	AY7	LPDDR3_CH1_DQB14	LPDDR3_CH1_DQB14 20
				DDR3L_CH1_DQ47 / LPDDR3_CH1_DQB15	BF5	LPDDR3_CH1_DQB15	LPDDR3_CH1_DQB15 20
				DDR3L_CH1_DQ48 / LPDDR3_CH1_DQB16	AU2	LPDDR3_CH1_DQB16	LPDDR3_CH1_DQB16 20
				DDR3L_CH1_DQ49 / LPDDR3_CH1_DQB17	AT10	LPDDR3_CH1_DQB17	LPDDR3_CH1_DQB17 20
				DDR3L_CH1_DQ50 / LPDDR3_CH1_DQB18	AT9	LPDDR3_CH1_DQB18	LPDDR3_CH1_DQB18 20
				DDR3L_CH1_DQ51 / LPDDR3_CH1_DQB19	AU1	LPDDR3_CH1_DQB19	LPDDR3_CH1_DQB19 20
				DDR3L_CH1_DQ52 / LPDDR3_CH1_DQB20	AY5	LPDDR3_CH1_DQB20	LPDDR3_CH1_DQB20 20
				DDR3L_CH1_DQ53 / LPDDR3_CH1_DQB21	AV5	LPDDR3_CH1_DQB21	LPDDR3_CH1_DQB21 20
				DDR3L_CH1_DQ54 / LPDDR3_CH1_DQB22	AV6	LPDDR3_CH1_DQB22	LPDDR3_CH1_DQB22 20
				DDR3L_CH1_DQ55 / LPDDR3_CH1_DQB23	AV7	LPDDR3_CH1_DQB23	LPDDR3_CH1_DQB23 20
				DDR3L_CH1_DQ56 / LPDDR3_CH1_DQB24	AY2	LPDDR3_CH1_DQB24	LPDDR3_CH1_DQB24 20
				DDR3L_CH1_DQ57 / LPDDR3_CH1_DQB25	BD2	LPDDR3_CH1_DQB25	LPDDR3_CH1_DQB25 20
				DDR3L_CH1_DQ58 / LPDDR3_CH1_DQB26	BD1	LPDDR3_CH1_DQB26	LPDDR3_CH1_DQB26 20
				DDR3L_CH1_DQ59 / LPDDR3_CH1_DQB27	BE2	LPDDR3_CH1_DQB27	LPDDR3_CH1_DQB27 20
				DDR3L_CH1_DQ60 / LPDDR3_CH1_DQB28	AW1	LPDDR3_CH1_DQB28	LPDDR3_CH1_DQB28 20
				DDR3L_CH1_DQ61 / LPDDR3_CH1_DQB29	AW2	LPDDR3_CH1_DQB29	LPDDR3_CH1_DQB29 20
				DDR3L_CH1_DQ62 / LPDDR3_CH1_DQB30	AY3	LPDDR3_CH1_DQB30	LPDDR3_CH1_DQB30 20
				DDR3L_CH1_DQ63 / LPDDR3_CH1_DQB31	BG2	LPDDR3_CH1_DQB31	LPDDR3_CH1_DQB31 20
20,22	LPDDR3_CH1_CLKB_N	LPDDR3_CH1_CLKB_N	BE19	DDR3L_CH1_CK0N / LPDDR3_CH1_CKN0B			
20,22	LPDDR3_CH1_CLKB_P	LPDDR3_CH1_CLKB_P	BD19	DDR3L_CH1_CKP0 / LPDDR3_CH1_CKP0B			
20,22	LPDDR3_CH1_CLKA_N	LPDDR3_CH1_CLKA_N	BD21	DDR3L_CH1_CKN1 / LPDDR3_CH1_CKN1A			
20,22	LPDDR3_CH1_CLKA_P	LPDDR3_CH1_CLKA_P	BB21	DDR3L_CH1_CKP1 / LPDDR3_CH1_CKP1A			
			BD23	DDR3L_CH1_DQSP8 / LPDDR3_CH1_NC			
			AR21	DDR3L_CH1_DSN0 / LPDDR3_CH1_NC			
			AT21	DDR3L_CH1_CB1 / LPDDR3_CH1_NC			
			AW23	DDR3L_CH1_CB2 / LPDDR3_CH1_NC			
			AW21	DDR3L_CH1_CB3 / LPDDR3_CH1_NC			
			BA19	DDR3L_CH1_CB4 / LPDDR3_CH1_NC			
			AW19	DDR3L_CH1_CB5 / LPDDR3_CH1_NC			
			BA23	DDR3L_CH1_CB6 / LPDDR3_CH1_NC			
			BB23	DDR3L_CH1_CB7 / LPDDR3_CH1_NC			
			BE23	DDR3L_CH1_DQSN8 / LPDDR3_CH1_NC			

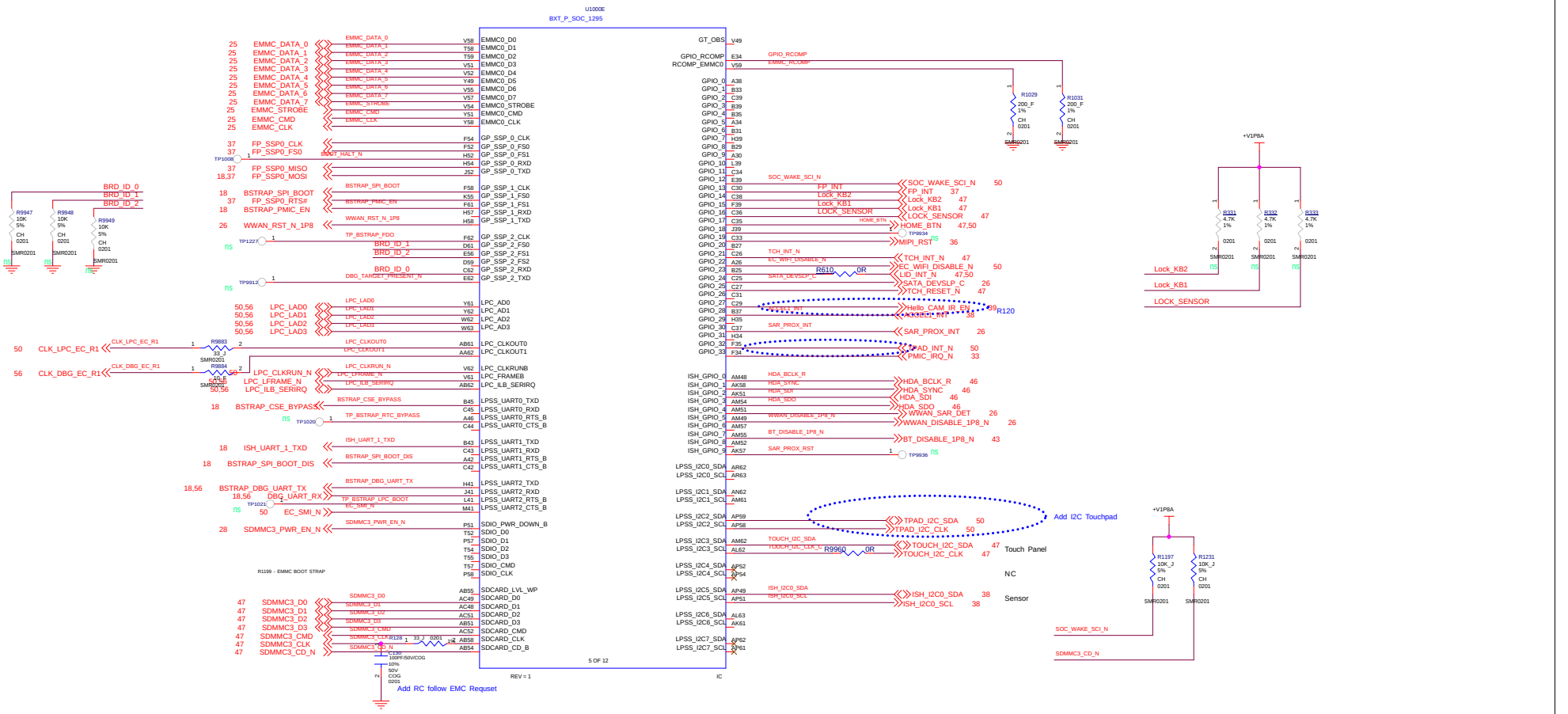
APOLLO LAKE			
Title: APOLLO LAKE			
Size: Custom	Document Number: LPDDR3-CPU		Rev: R100
Date: Tuesday, December 06, 2016	Sheet 4 of 57		



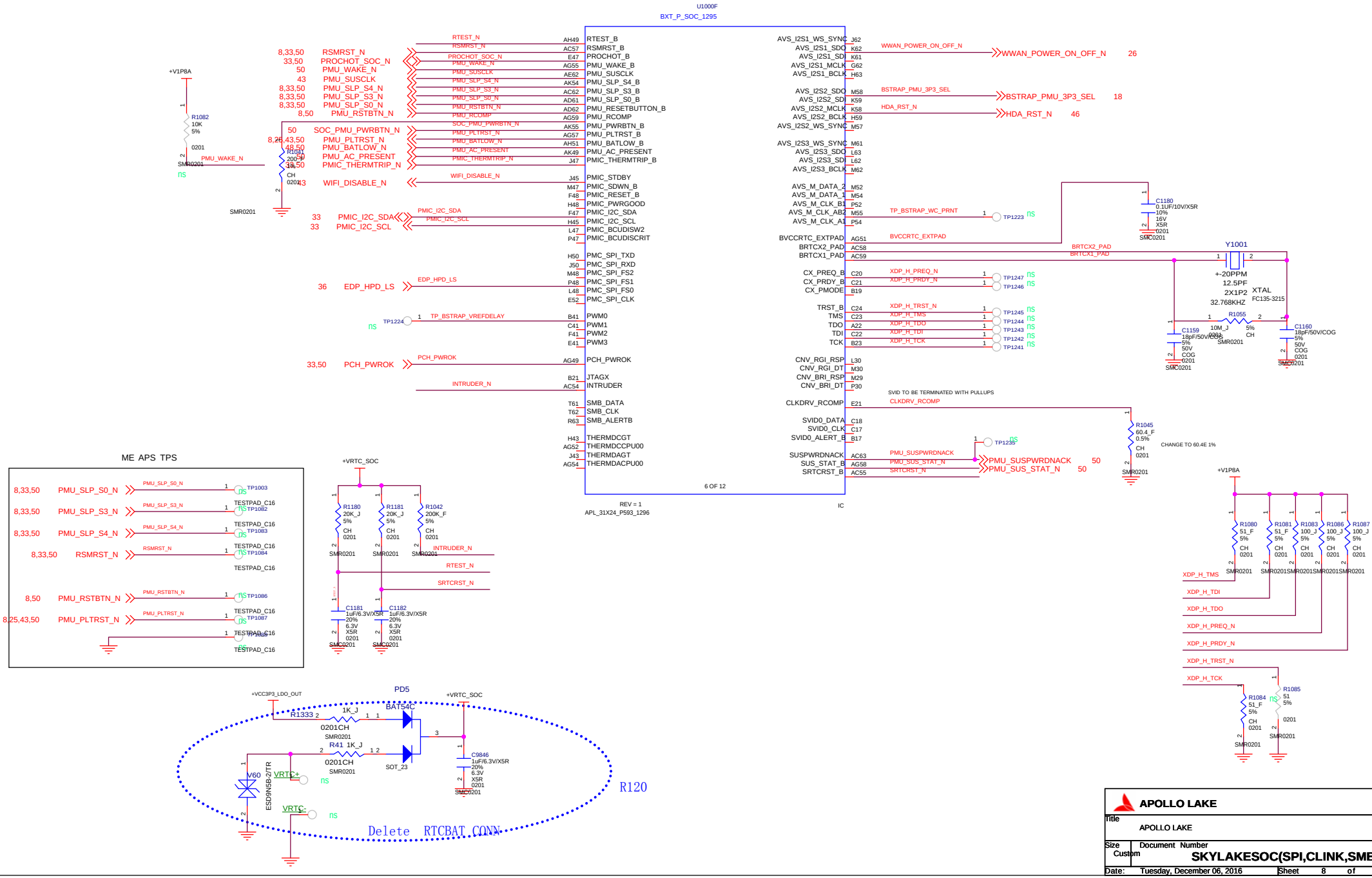
APOLLO LAKE			
Title: APOLLO LAKE			
Size: Custom	Document Number: SKYLAKE SOC (DISPLAY)		Rev: R100
Date: Tuesday, December 06, 2016	Sheet 5 of 57		



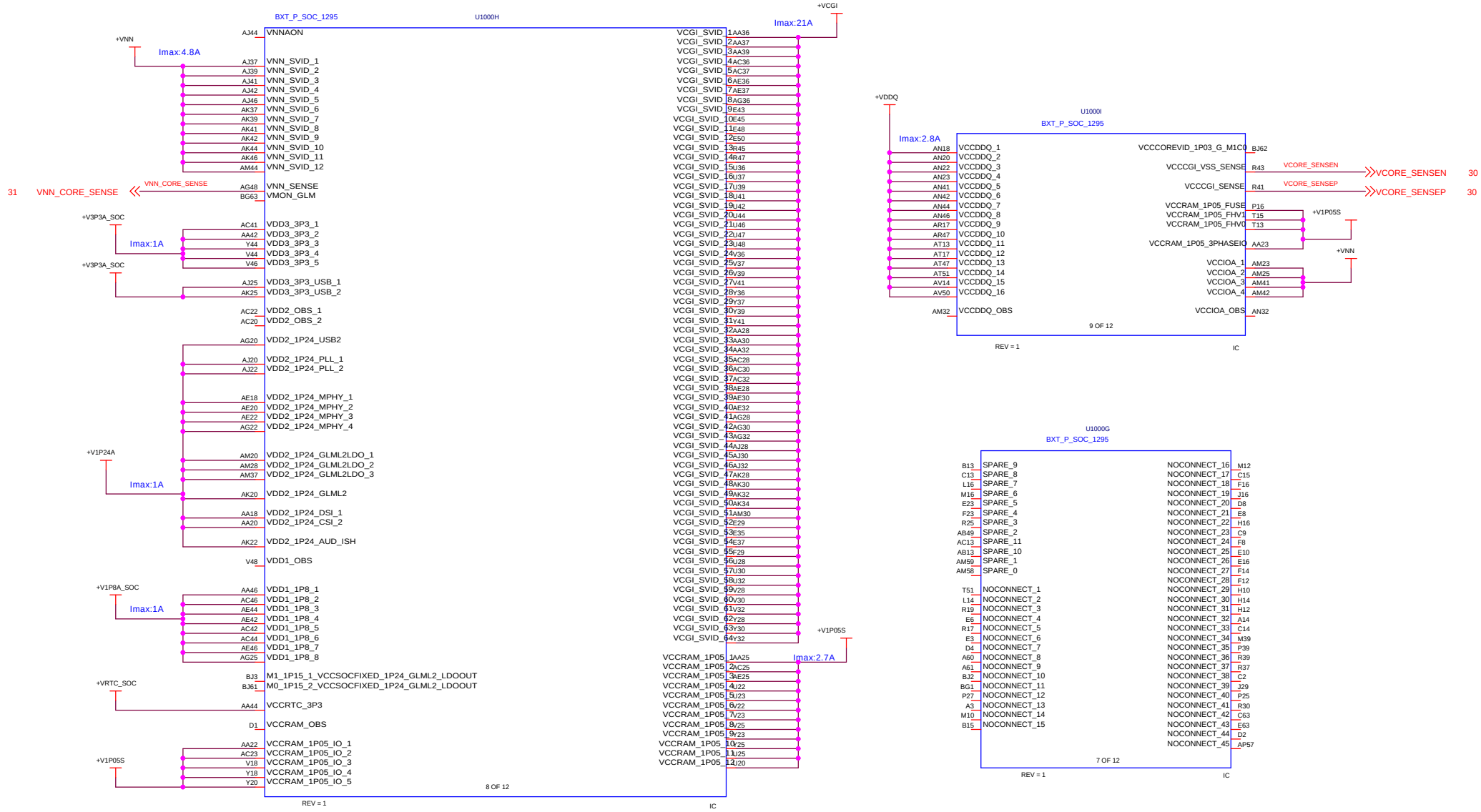
Title	APOLLO LAKE
Size	Custom
Document Number	SKYLAKE SOC (PCIE,SATA,USB)
Rev	R100
Date:	Tuesday, December 06, 2016
Sheet	6 of 57

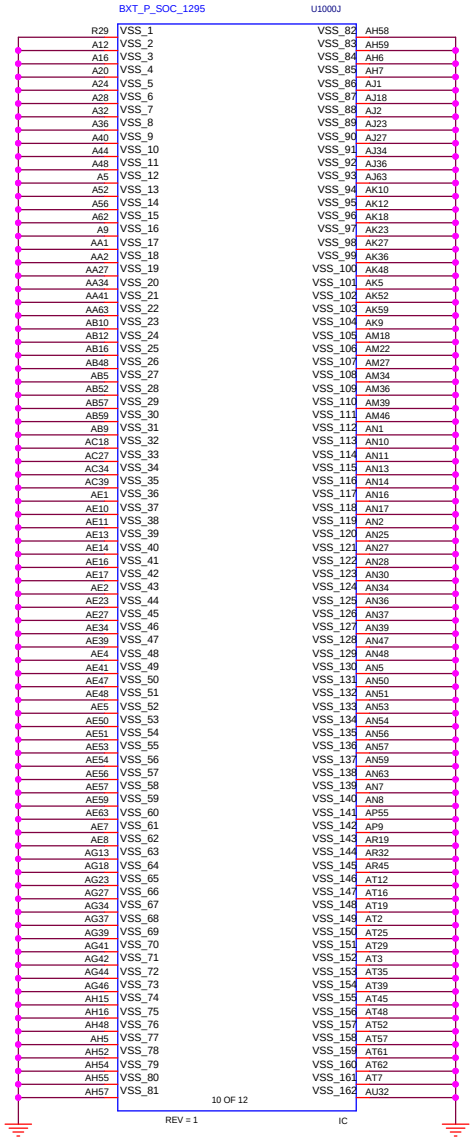


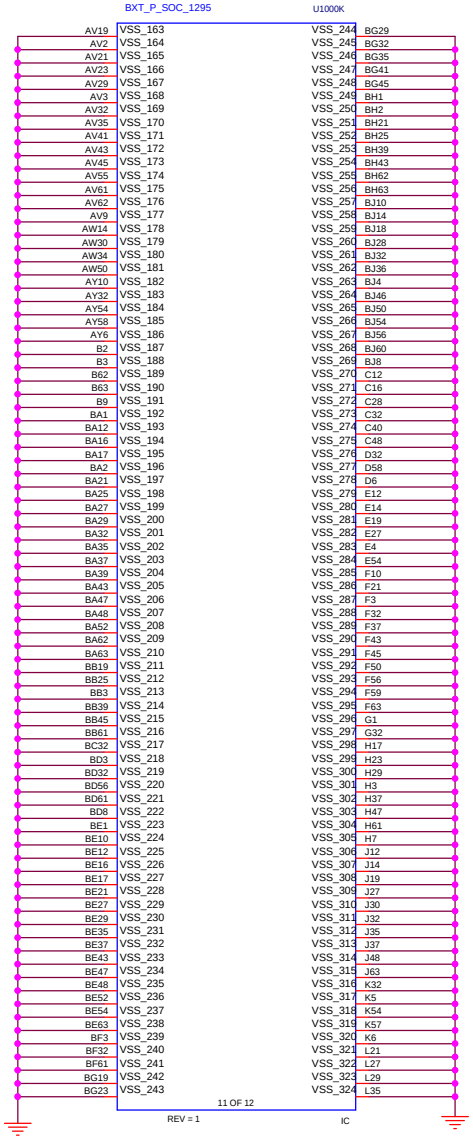
Title	APOLLO LAKE
Size	C
Document Number	SKYLAKE SOC (CSI-MIPI,EMMC)
Rev	R100
Date:	Tuesday, December 06, 2016
Sheet	7 of 57

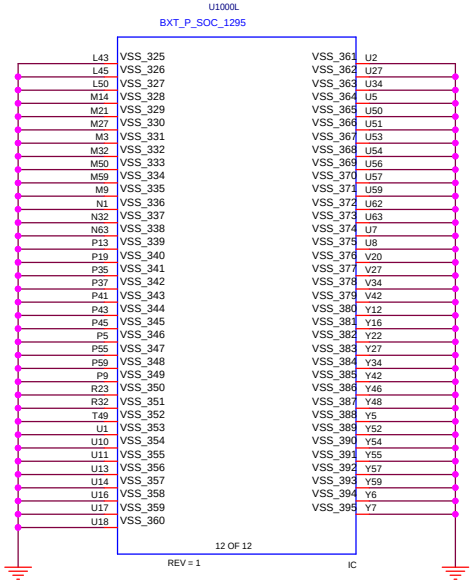


Title	APOLLO LAKE
	APOLLO LAKE
Size	Custom
Document Number	SKYLAKESOC(SPI,CLINK,SMBUS)
Rev	R100
Date:	Tuesday, December 06, 2016
Sheet	8 of 57


BXT_P_SOC_1295
U1000H
+VNN
Imax:4.8A
VNNAON
VNN_SVID_1
VNN_SVID_2
VNN_SVID_3
VNN_SVID_4
VNN_SVID_5
VNN_SVID_6
VNN_SVID_7
VNN_SVID_8
VNN_SVID_9
VNN_SVID_10
VNN_SVID_11
VNN_SVID_12
VNN_CORE_SENSE
VNN_SENSE
VMON_GLM
31
+V3P3A_SOC
Imax:1A
VDD3_3P3_1
VDD3_3P3_2
VDD3_3P3_3
VDD3_3P3_4
VDD3_3P3_5
VDD3_3P3_USB_1
VDD3_3P3_USB_2
VDD2_OBS_1
VDD2_OBS_2
VDD2_1P24_USB2
VDD2_1P24_PLL_1
VDD2_1P24_PLL_2
VDD2_1P24_MPHY_1
VDD2_1P24_MPHY_2
VDD2_1P24_MPHY_3
VDD2_1P24_MPHY_4
+V1P24A
Imax:1A
VDD2_1P24_GLML2LDO_1
VDD2_1P24_GLML2LDO_2
VDD2_1P24_GLML2LDO_3
VDD2_1P24_GLML2
VDD2_1P24_DSI_1
VDD2_1P24_CSI_2
VDD2_1P24_AUD_ISH
VDD1_OBS
+V1P8A_SOC
Imax:1A
VDD1_1P8_1
VDD1_1P8_2
VDD1_1P8_3
VDD1_1P8_4
VDD1_1P8_5
VDD1_1P8_6
VDD1_1P8_7
VDD1_1P8_8
+VRTC_SOC
M1_1P15_1_VCCSOCFIXED_1P24_GLML2_LDOOUT
M0_1P15_2_VCCSOCFIXED_1P24_GLML2_LDOOUT
VCCRTC_3P3
VCCRAM_OBS
+V1P05S
VCCRAM_1P05_IO_1
VCCRAM_1P05_IO_2
VCCRAM_1P05_IO_3
VCCRAM_1P05_IO_4
VCCRAM_1P05_IO_5
8 OF 12
REV = 1
IC
+VCGI
Imax:21A
VCGI_SVID_1
VCGI_SVID_2
VCGI_SVID_3
VCGI_SVID_4
VCGI_SVID_5
VCGI_SVID_6
VCGI_SVID_7
VCGI_SVID_8
VCGI_SVID_9
VCGI_SVID_10
VCGI_SVID_11
VCGI_SVID_12
VCGI_SVID_13
VCGI_SVID_14
VCGI_SVID_15
VCGI_SVID_16
VCGI_SVID_17
VCGI_SVID_18
VCGI_SVID_19
VCGI_SVID_20
VCGI_SVID_21
VCGI_SVID_22
VCGI_SVID_23
VCGI_SVID_24
VCGI_SVID_25
VCGI_SVID_26
VCGI_SVID_27
VCGI_SVID_28
VCGI_SVID_29
VCGI_SVID_30
VCGI_SVID_31
VCGI_SVID_32
VCGI_SVID_33
VCGI_SVID_34
VCGI_SVID_35
VCGI_SVID_36
VCGI_SVID_37
VCGI_SVID_38
VCGI_SVID_39
VCGI_SVID_40
VCGI_SVID_41
VCGI_SVID_42
VCGI_SVID_43
VCGI_SVID_44
VCGI_SVID_45
VCGI_SVID_46
VCGI_SVID_47
VCGI_SVID_48
VCGI_SVID_49
VCGI_SVID_50
VCGI_SVID_51
VCGI_SVID_52
VCGI_SVID_53
VCGI_SVID_54
VCGI_SVID_55
VCGI_SVID_56
VCGI_SVID_57
VCGI_SVID_58
VCGI_SVID_59
VCGI_SVID_60
VCGI_SVID_61
VCGI_SVID_62
VCGI_SVID_63
VCGI_SVID_64
+V1P05S
Imax:2.7A
VCCRAM_1P05_1
VCCRAM_1P05_2
VCCRAM_1P05_3
VCCRAM_1P05_4
VCCRAM_1P05_5
VCCRAM_1P05_6
VCCRAM_1P05_7
VCCRAM_1P05_8
VCCRAM_1P05_9
VCCRAM_1P05_10
VCCRAM_1P05_11
VCCRAM_1P05_12
+VDDQ
U1000I
BXT_P_SOC_1295
Imax:2.8A
VCCDDQ_1
VCCDDQ_2
VCCDDQ_3
VCCDDQ_4
VCCDDQ_5
VCCDDQ_6
VCCDDQ_7
VCCDDQ_8
VCCDDQ_9
VCCDDQ_10
VCCDDQ_11
VCCDDQ_12
VCCDDQ_13
VCCDDQ_14
VCCDDQ_15
VCCDDQ_16
VCCDDQ_OBS
VCCCOREVID_1P03_G_M1C0
VCCCGI_VSS_SENSE
VCCCGI_SENSE
VCCRAM_1P05_FUSE
VCCRAM_1P05_FHV1
VCCRAM_1P05_FHV0
VCCRAM_1P05_3PHASEIO
VCCIOA_1
VCCIOA_2
VCCIOA_3
VCCIOA_4
VCCIOA_OBS
VCORE_SENSEN
VCORE_SENSEP
30
+V1P05S
+VNN
9 OF 12
REV = 1
IC
U1000G
BXT_P_SOC_1295
SPARE_9
SPARE_8
SPARE_7
SPARE_6
SPARE_5
SPARE_4
SPARE_3
SPARE_2
SPARE_11
SPARE_10
SPARE_1
SPARE_0
NOCONNECT_1
NOCONNECT_2
NOCONNECT_3
NOCONNECT_4
NOCONNECT_5
NOCONNECT_6
NOCONNECT_7
NOCONNECT_8
NOCONNECT_9
NOCONNECT_10
NOCONNECT_11
NOCONNECT_12
NOCONNECT_13
NOCONNECT_14
NOCONNECT_15
NOCONNECT_16
NOCONNECT_17
NOCONNECT_18
NOCONNECT_19
NOCONNECT_20
NOCONNECT_21
NOCONNECT_22
NOCONNECT_23
NOCONNECT_24
NOCONNECT_25
NOCONNECT_26
NOCONNECT_27
NOCONNECT_28
NOCONNECT_29
NOCONNECT_30
NOCONNECT_31
NOCONNECT_32
NOCONNECT_33
NOCONNECT_34
NOCONNECT_35
NOCONNECT_36
NOCONNECT_37
NOCONNECT_38
NOCONNECT_39
NOCONNECT_40
NOCONNECT_41
NOCONNECT_42
NOCONNECT_43
NOCONNECT_44
NOCONNECT_45
7 OF 12
REV = 1
IC
APOLLO LAKE
Title
APOLLO LAKE
Size
Custom
Document Number
SKYLAKE SOC(LPSS,ISH,AUDIO)
Rev
R100
Date:
Tuesday, December 06, 2016
Sheet
9
of
57



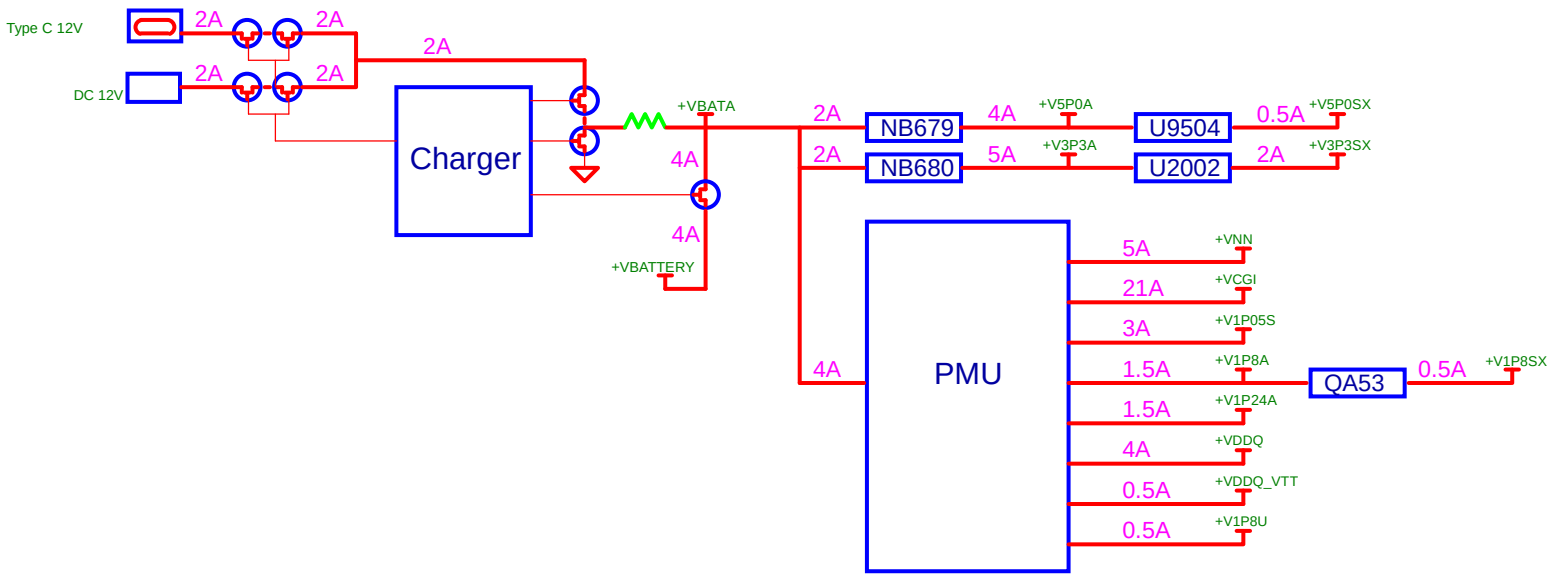




APOLLO LAKE

Title	APOLLO LAKE	
Size: Custom	Document Number: SKYLAKE SOC(CLOCKS,PWRMGMT)	Rev: R100
Date: Tuesday, December 06, 2016	Sheet 10 of 57	

Power Deliver



APOLLO LAKE		
Title: APOLLO LAKE		
Size: Custom	Document Number: SKYLAKE SOC (POWER-CORE,GT)	Rev: R100
Date: Tuesday, December 06, 2016	Sheet 11 of 57	

BLANK

BLANK

APOLLO LAKE

Title: APOLLO LAKE		
Size: Custom	Document Number: SKYLAKE SOC (PCH POWER)	Rev: R100
Date: Tuesday, December 06, 2016	Sheet 13 of 57	

BLANK

APOLLO LAKE

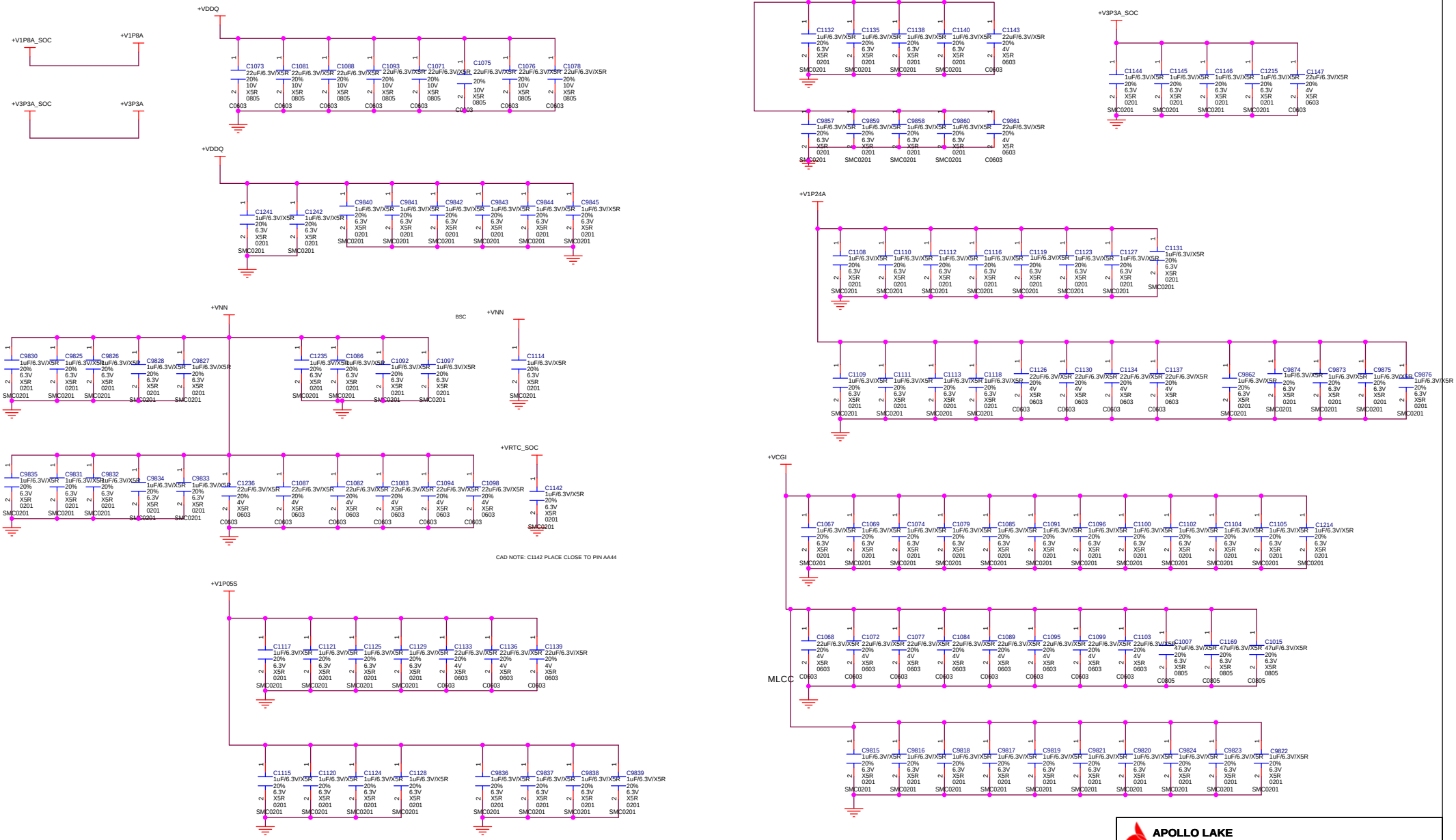
Title: APOLLO LAKE		
Size: Custom	Document Number: SKYLAKE SOC (CPU MISC,JTAG)	Rev: R100
Date: Tuesday, December 06, 2016	Sheet 14 of 57	

BLANK

BLANK

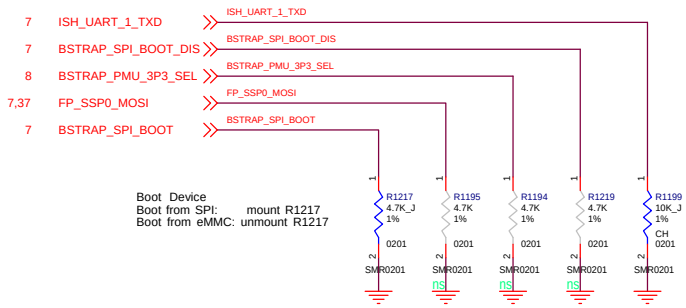
APOLLO LAKE

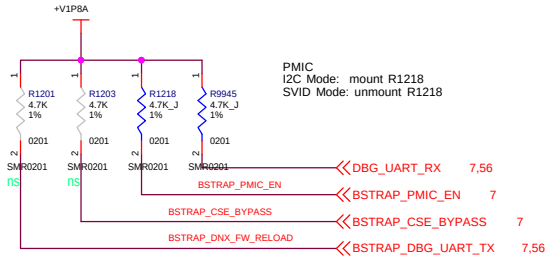
Title: APOLLO LAKE		
Size: Custom	Document Number: SKYLAKE SOC (GND)	Rev: R100
Date: Tuesday, December 06, 2016	Sheet 16 of 57	



APOLLO LAKE

Title	APOLLO LAKE	
Size: Custom	Document Number: SKYLAKE SOC (DECOUPLING)	Rev: R100
Date: Tuesday, December 06, 2016	Sheet 17 of 57	



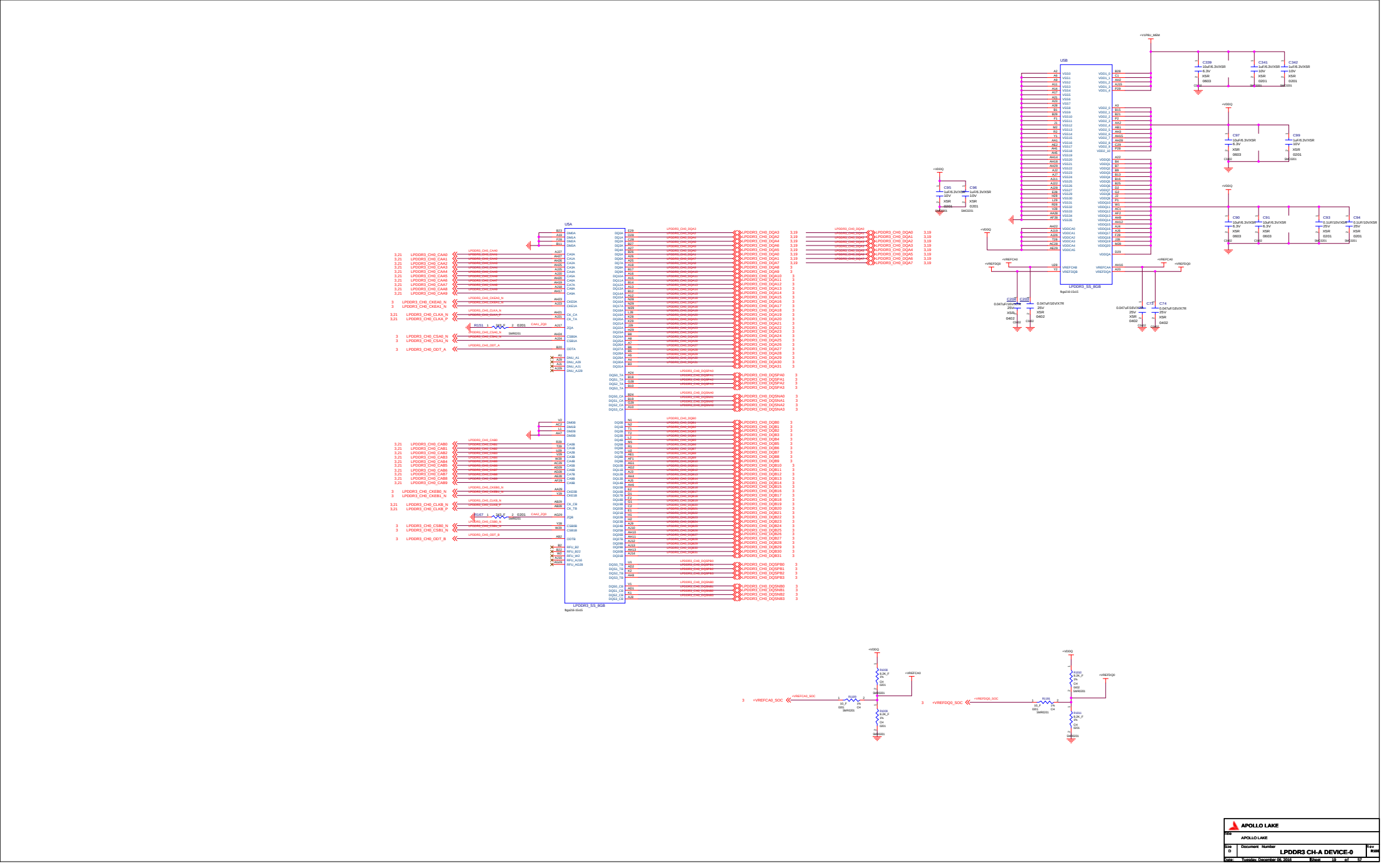


APOLLO LAKE

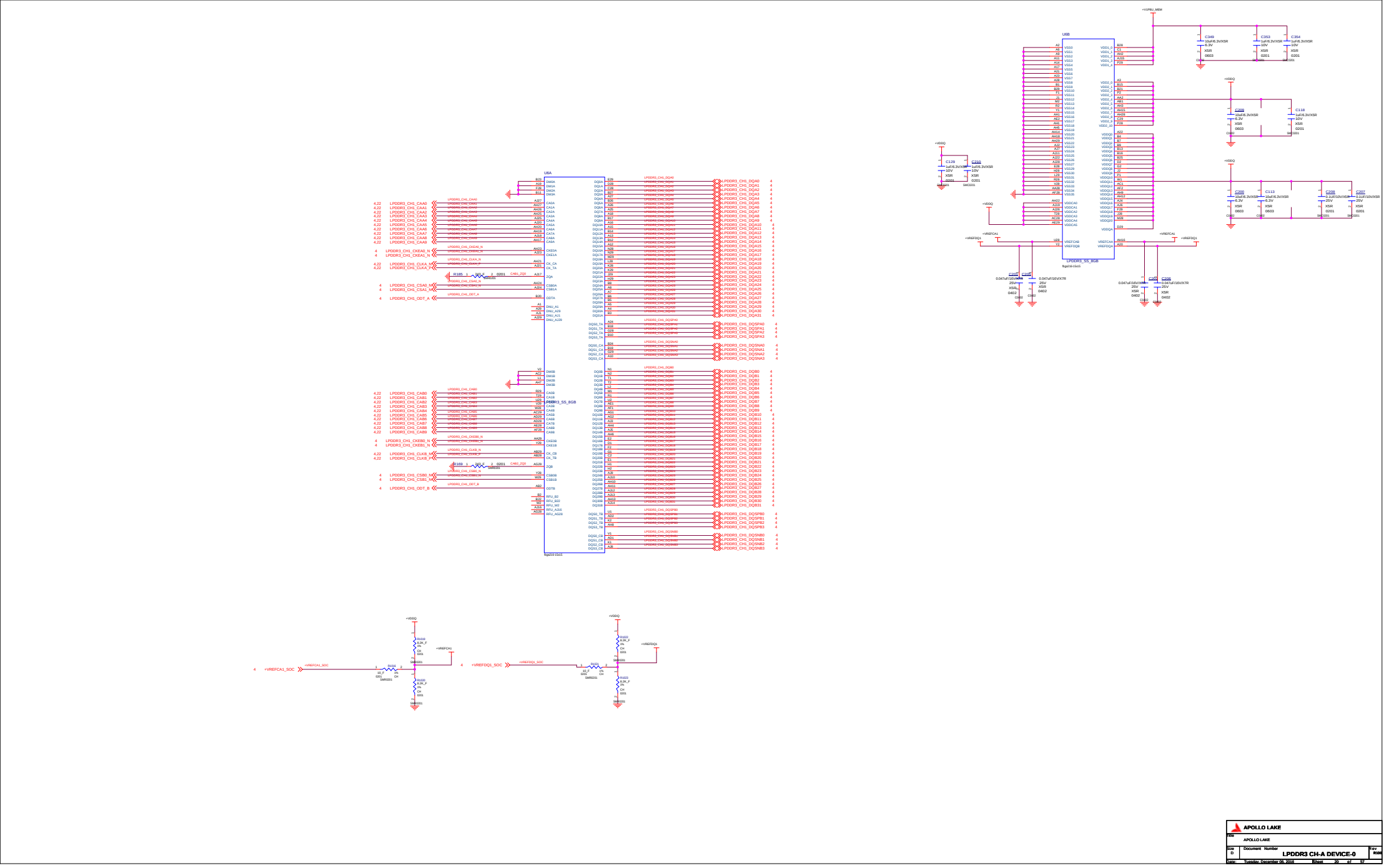
Title: APOLLO LAKE

Size: Custom | Document Number: SKYLAKE SOC (DECOUPLING) | Rev: R100

Date: Tuesday, December 06, 2016 | Sheet 18 of 57

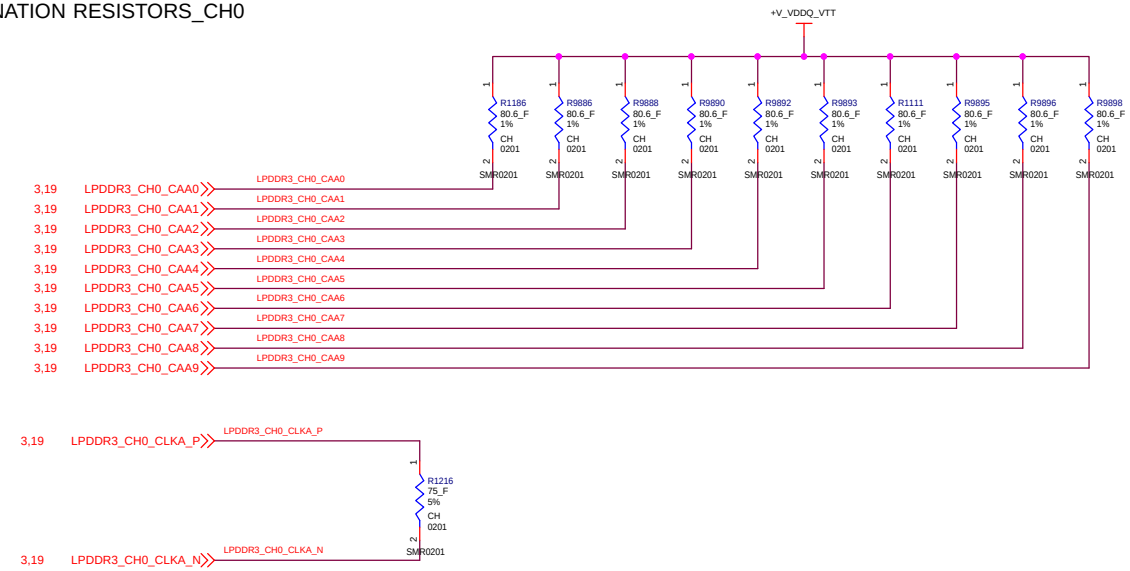


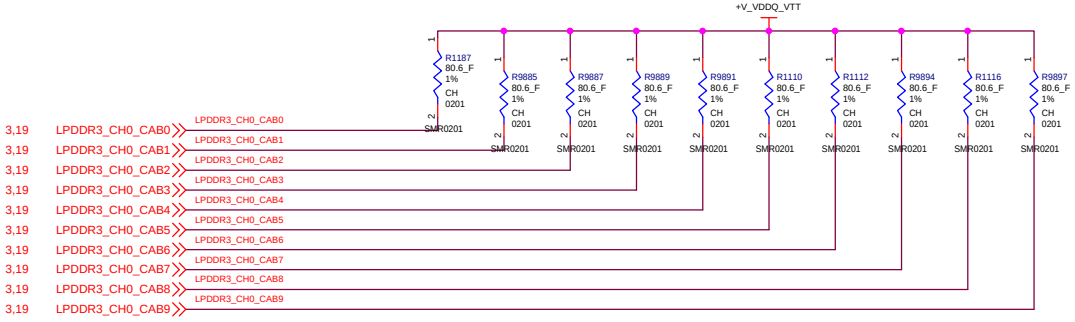
APOLLO LAKE			
File: APOLLO LAKE			
Size: D	Document Number: LPDDR3 CH-A DEVICE-0		Rev: R058
Date: Tuesday, December 06, 2016	Sheet: 19 of 57		



APOLLO LAKE			
Title: APOLLO LAKE			
Size: D	Document Number: LPDDR3 CH-A DEVICE-0		Rev: R098
Date: Tuesday, December 06, 2016	Sheet: 30 of 57		

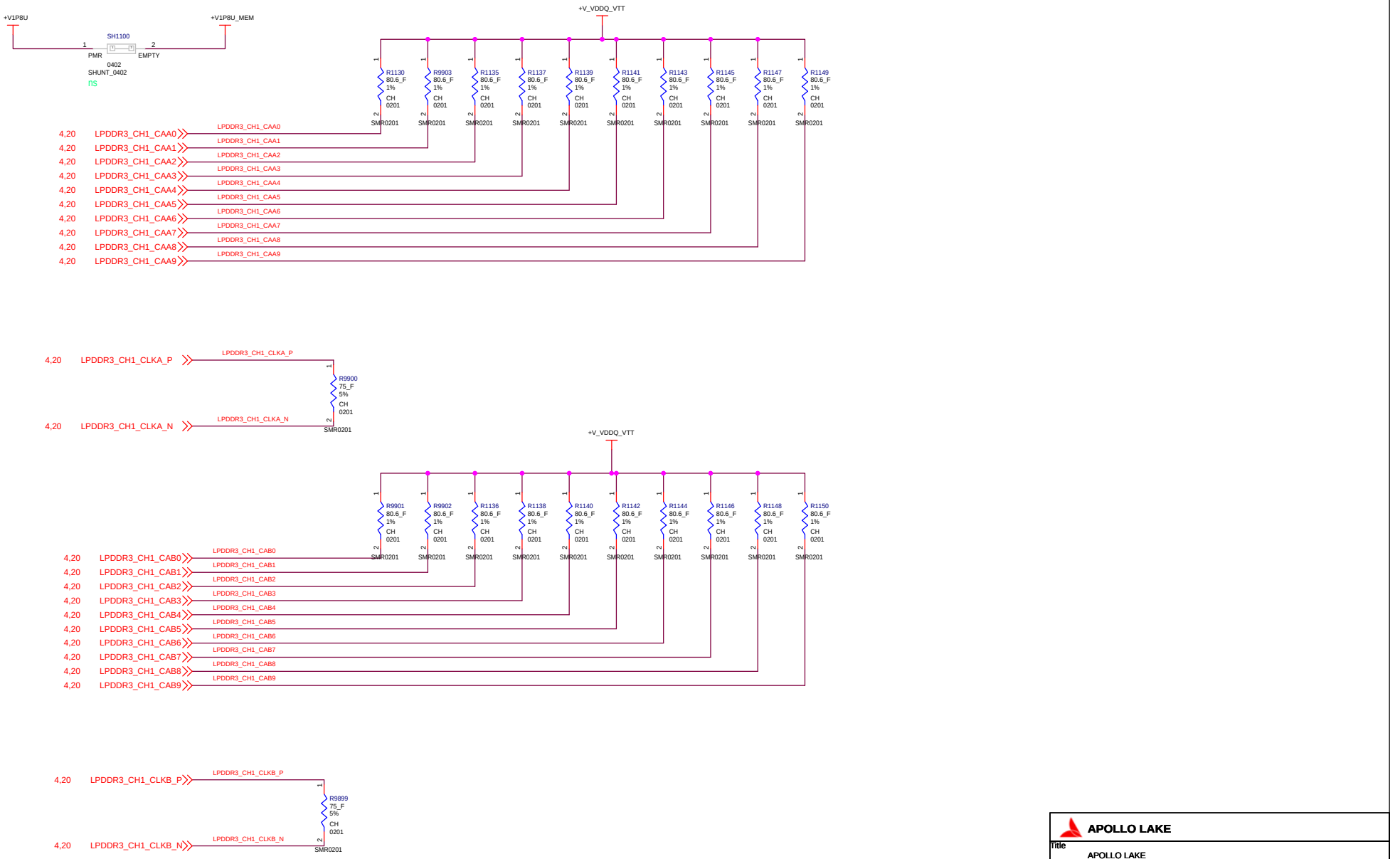
LPDDR3L-RS TERMINATION RESISTORS_CH0



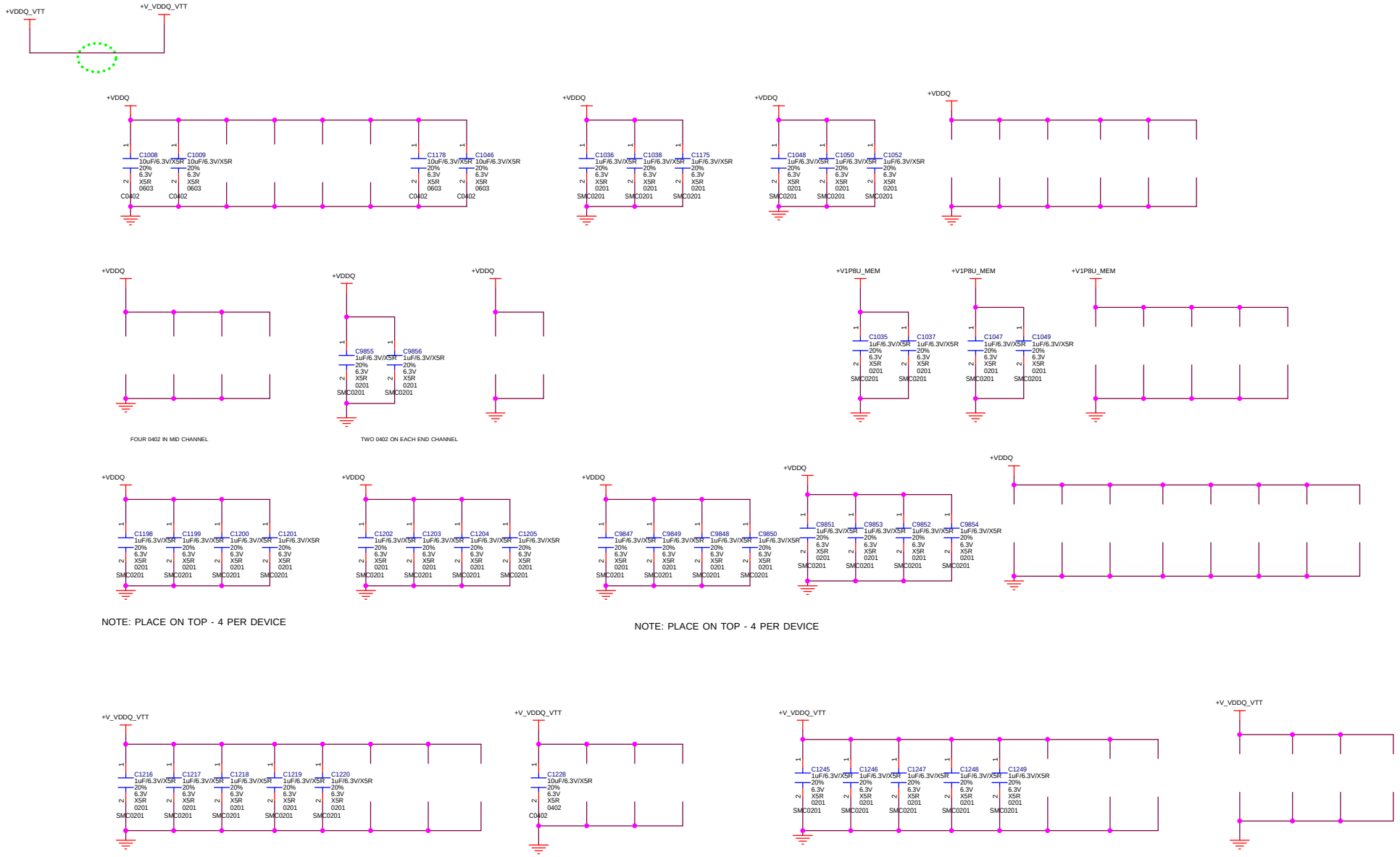


APOLLO LAKE			
Title: APOLLO LAKE			
Size: Custom	Document Number: LPDDR3 CH-A DEVICE-1		Rev: R100
Date: Tuesday, December 06, 2016	Sheet 21 of 57		

LPDDR3L-RS TERMINATION RESISTORS_CH1



APOLLO LAKE		
Title: APOLLO LAKE		
Size: Custom	Document Number: LPDDR3 CH-A DEVICE-1	Rev: R100
Date: Tuesday, December 06, 2016	Sheet 22 of 57	

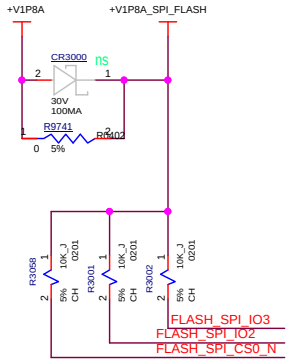


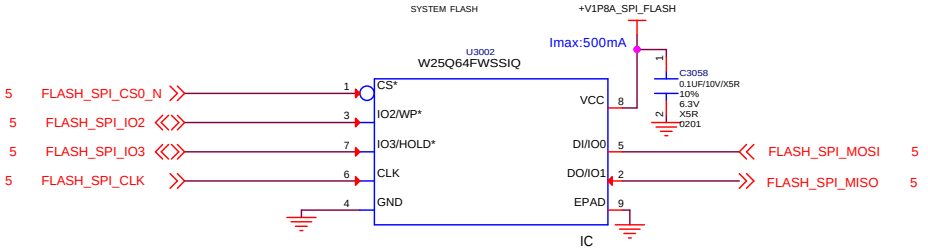
APOLLO LAKE

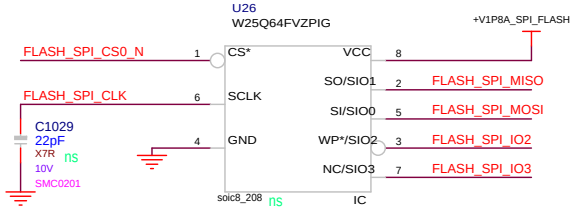
Title: APOLLO LAKE

Size: Custom | Document Number: LPDDR3 DECOUPLING | Rev: R100

Date: Tuesday, December 06, 2016 | Sheet 23 of 57

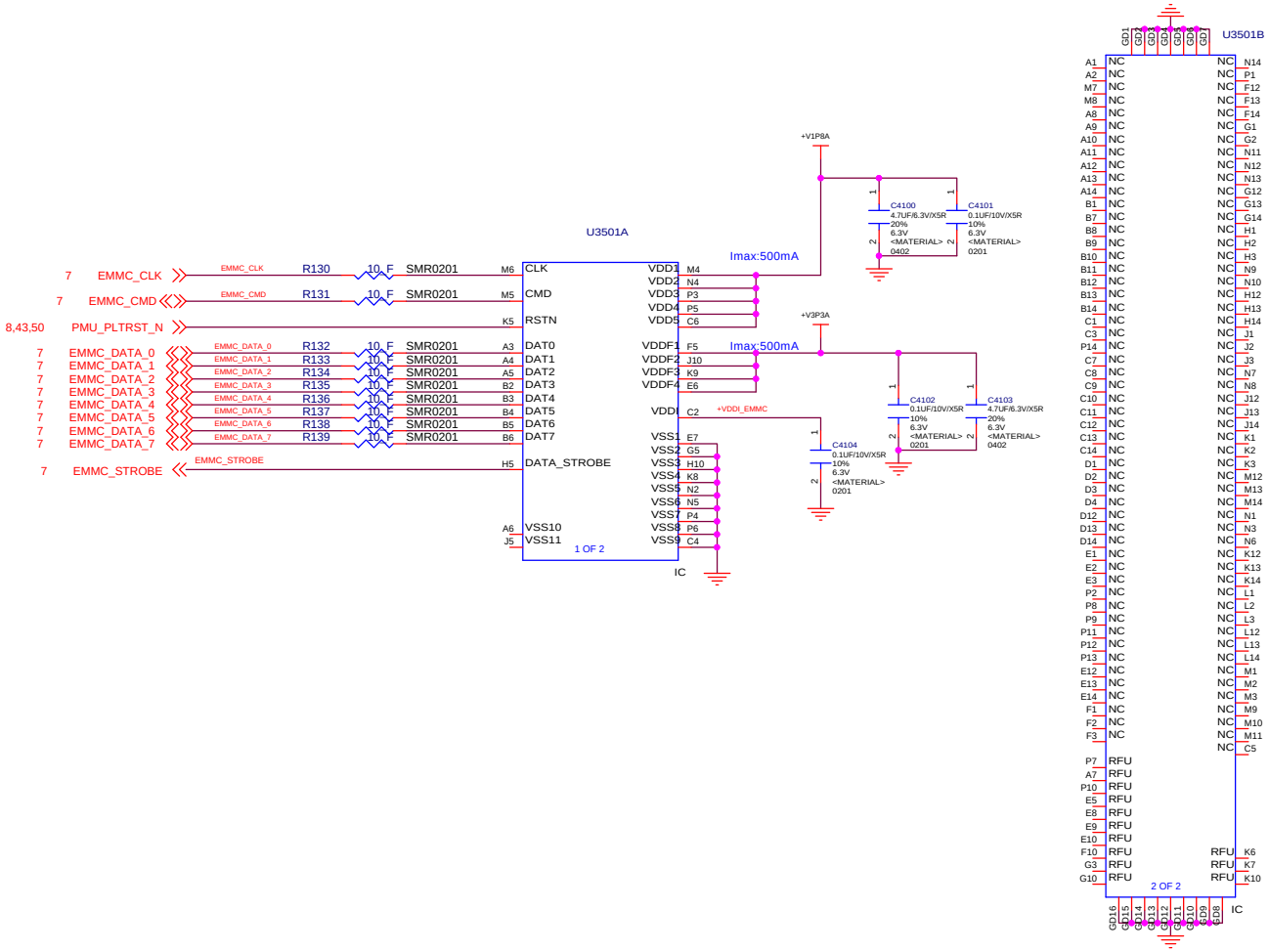




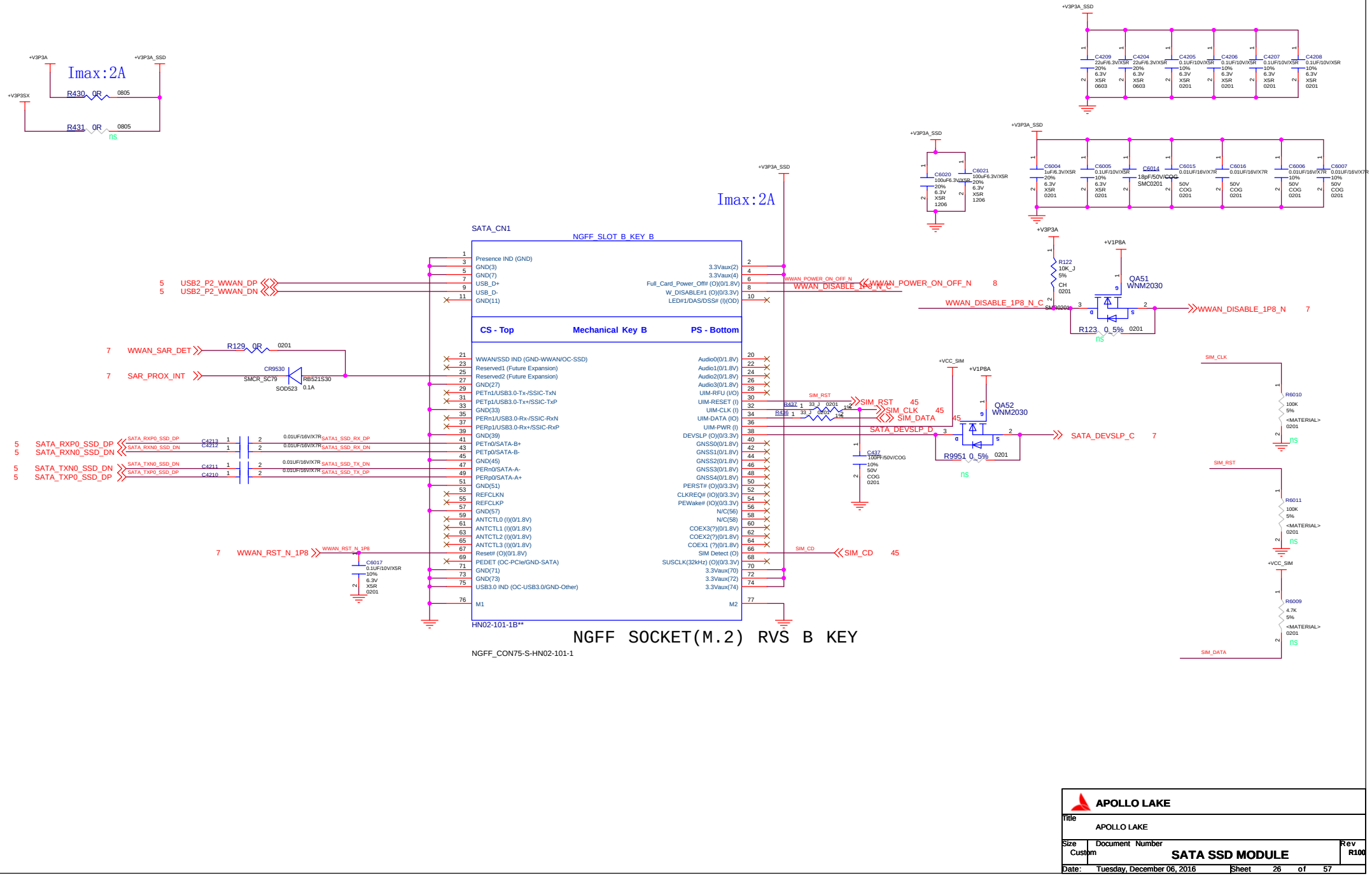


APOLLO LAKE

Title: APOLLO LAKE		
Size: B	Document Number: LPDDR3 DECOUPLING	Rev: R100
Date: Tuesday, December 06, 2016	Sheet 24 of 57	



APOLLO LAKE			
Title: APOLLO LAKE			
Size: Custom	Document Number: EMMC		Rev: R100
Date: Tuesday, December 06, 2016	Sheet 25 of 57		



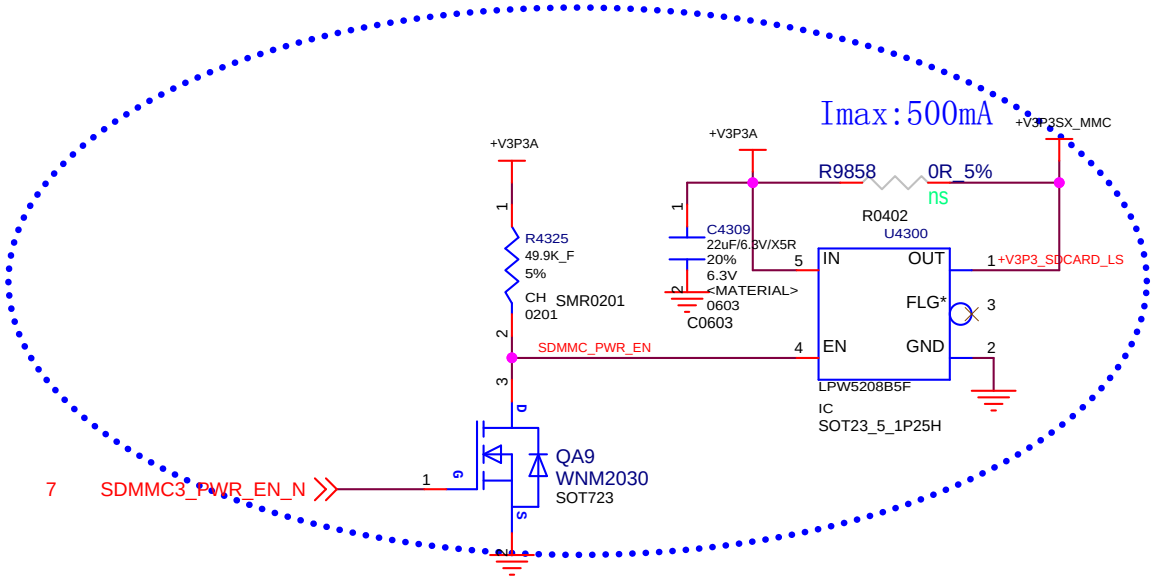
APOLLO LAKE			
Title: APOLLO LAKE			
Size: Custom	Document Number: SATA SSD MODULE		Rev: R100
Date: Tuesday, December 06, 2016	Sheet 26 of 57		

APOLLO LAKE

Title: APOLLO LAKE

Size: B | Document Number: MICRO-SD CARD | Rev: R100

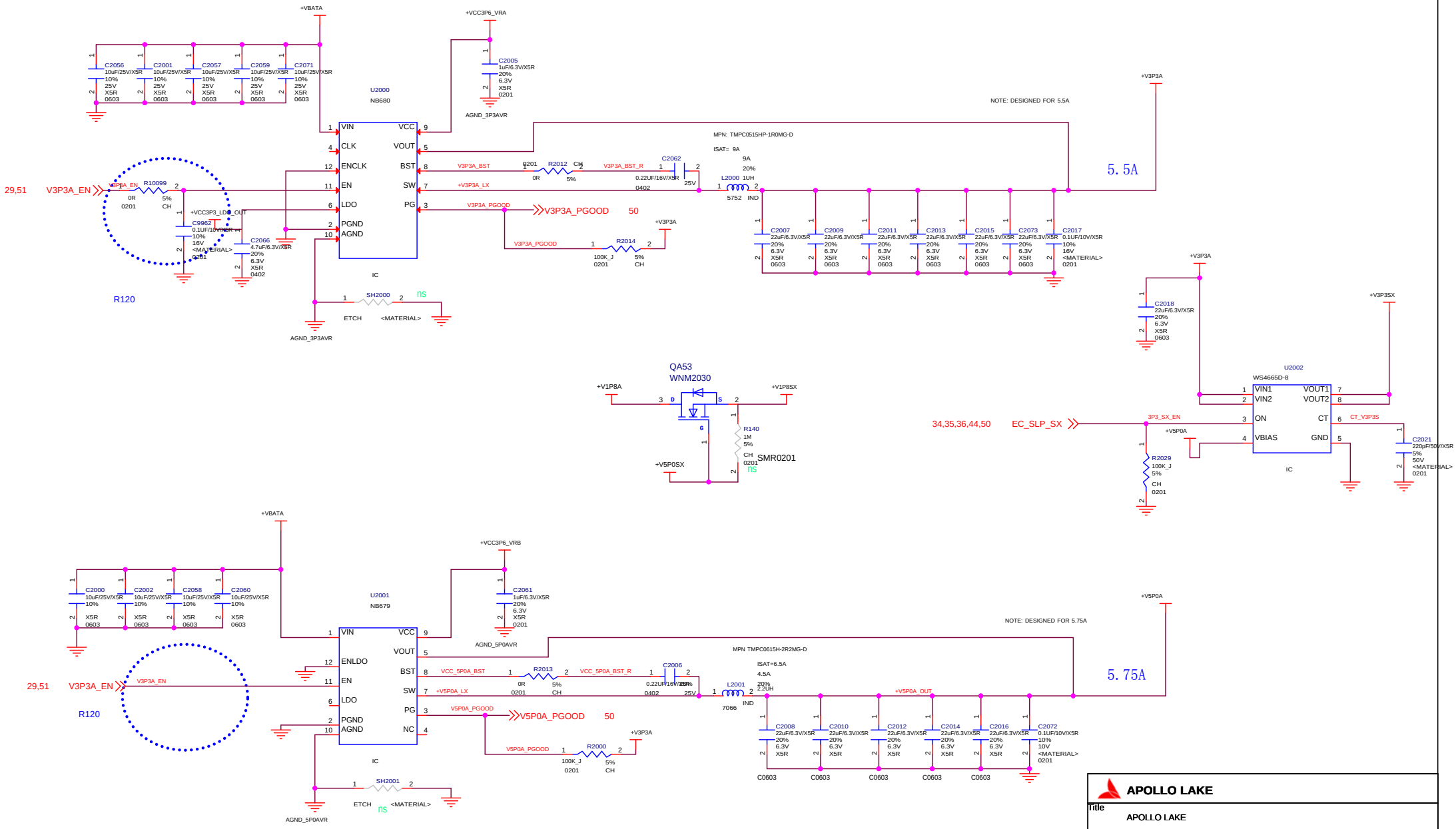
Date: Tuesday, December 06, 2016 | Sheet 27 of 57



R120

Use USB2.0 transfer to TF ,R9858 Install,U4300 NS

APOLLO LAKE		
Title: APOLLO LAKE		
Size: A	Document Number: SDCARD POWER	Rev: R100
Date: Tuesday, December 06, 2016	Sheet 28 of 57	



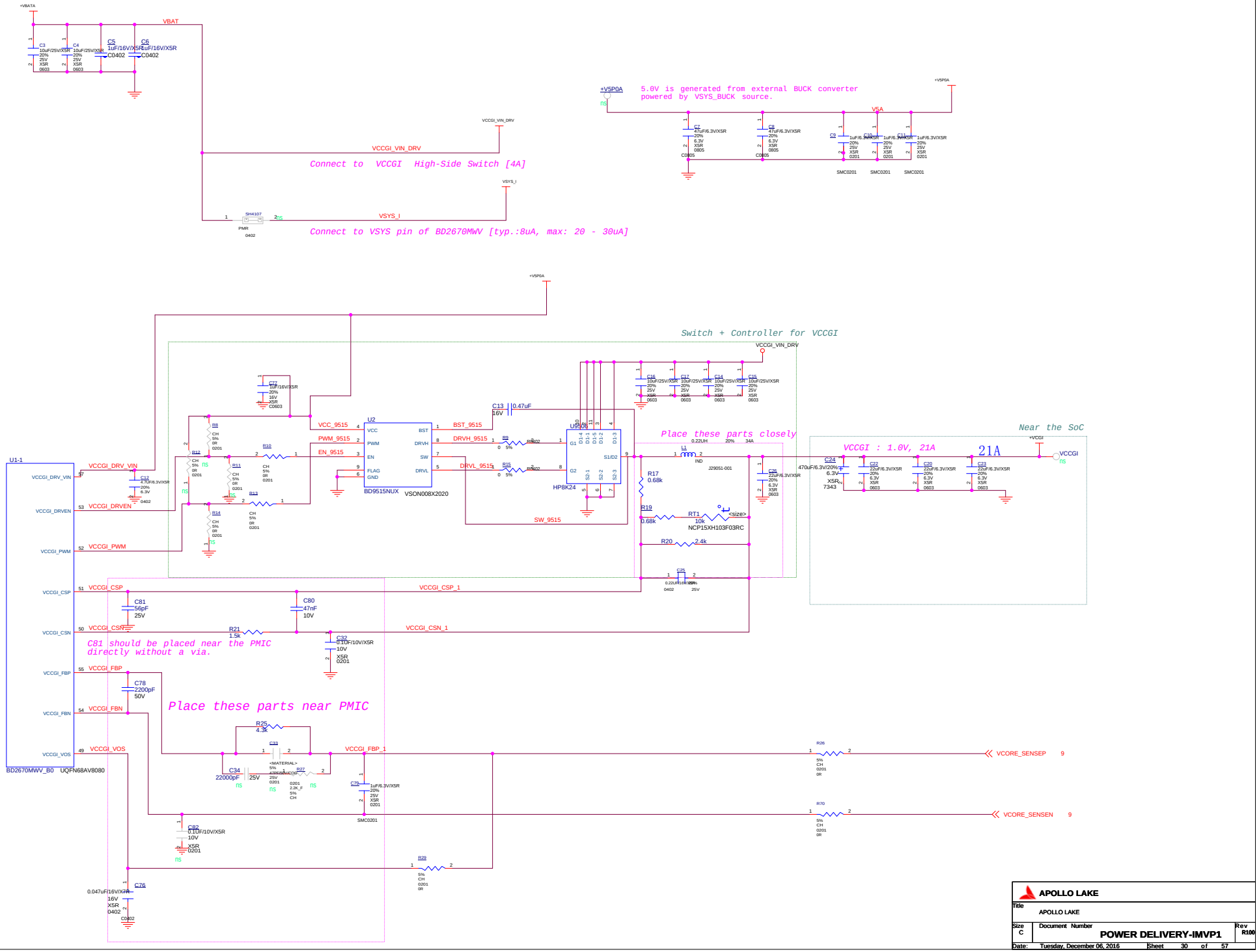
APOLLO LAKE

Title: APOLLO LAKE

Size: Custom | Document Number: POWER DELIVERY 5V AND 3.3V | Rev: R100

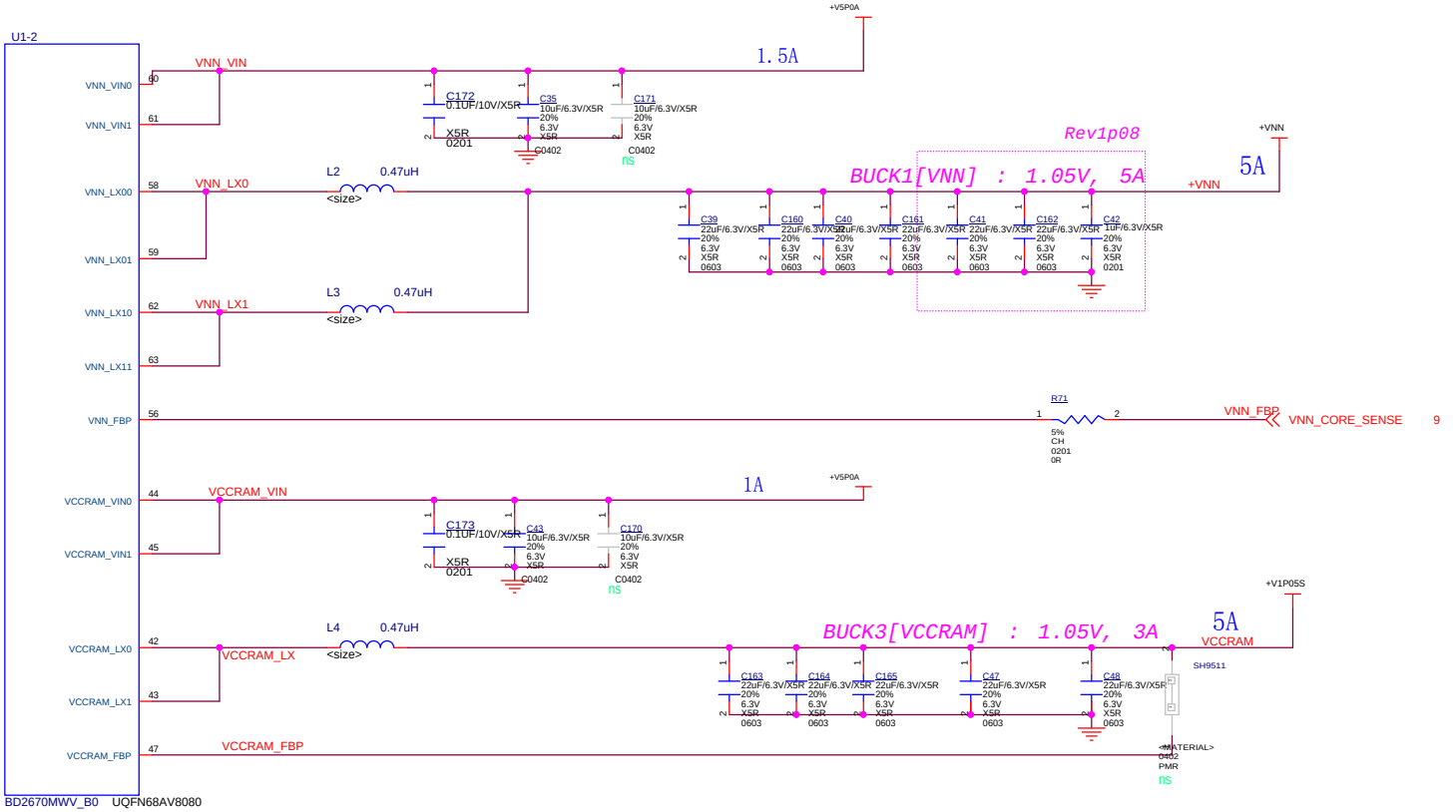
Date: Tuesday, December 06, 2016 | Sheet 29 of 57

2S/3S battery input [5.4V to 21V]



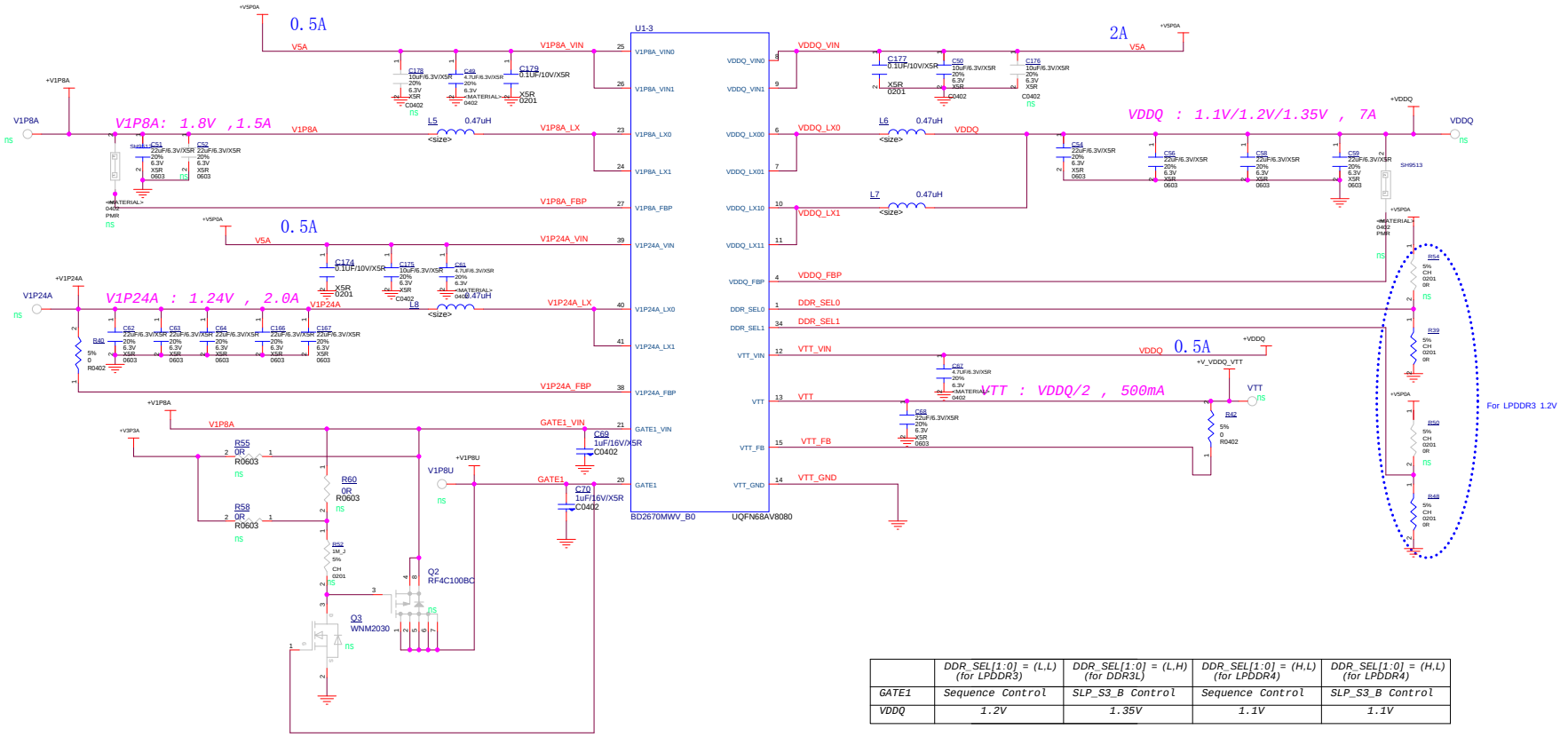
APOLLO LAKE		
Title: APOLLO LAKE		
Size: C	Document Number: POWER DELIVERY-IMVP1	Rev: R100
Date: Tuesday, December 06, 2016	Sheet 30 of 57	

VNN[BUCK1], VCCRAM[BUCK3]



APOLLO LAKE		
Title: APOLLO LAKE		
Size: Custom	Document Number: POWER DELIVERY-IMVP2	Rev: R100
Date: Tuesday, December 06, 2016	Sheet 31 of 57	

V1P8A[BUCK4], V1P24A[BUCK5],VDDQ[BUCK6]



	DDR_SEL[1:0] = (L,L) (for LPDDR3)	DDR_SEL[1:0] = (L,H) (for DDR3L)	DDR_SEL[1:0] = (H,L) (for LPDDR4)	DDR_SEL[1:0] = (H,L) (for LPDDR4)
GATE1	Sequence Control	SLP_S3_B Control	Sequence Control	SLP_S3_B Control
VDDQ	1.2V	1.35V	1.1V	1.1V

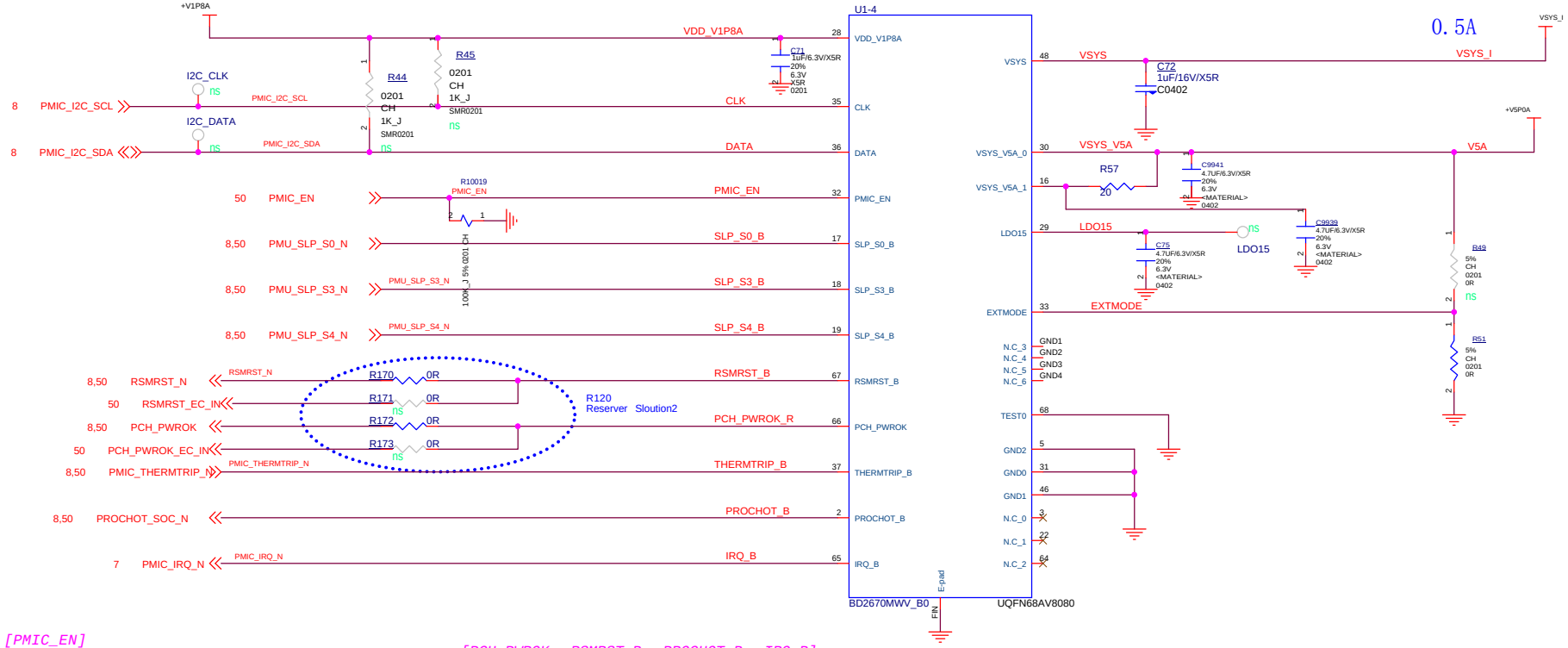
APOLLO LAKE

Title: APOLLO LAKE

Size: C | Document Number: POWER DELIVERY 1.2V | Rev: R100

Date: Tuesday, December 06, 2016 | Sheet 32 of 57

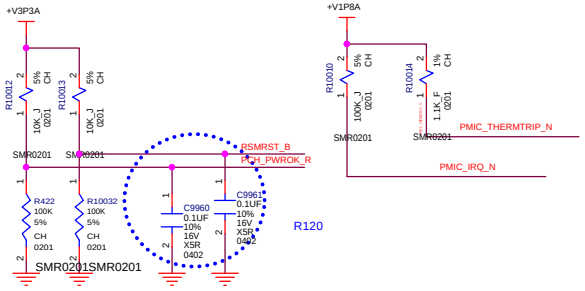
I2C , Other signals



[PMIC_EN]
Connected to EC.

[SLP_S0_B, SLP_S3_B, SLP_S4_B, THERMTRIP_B]
Connected to SoC.

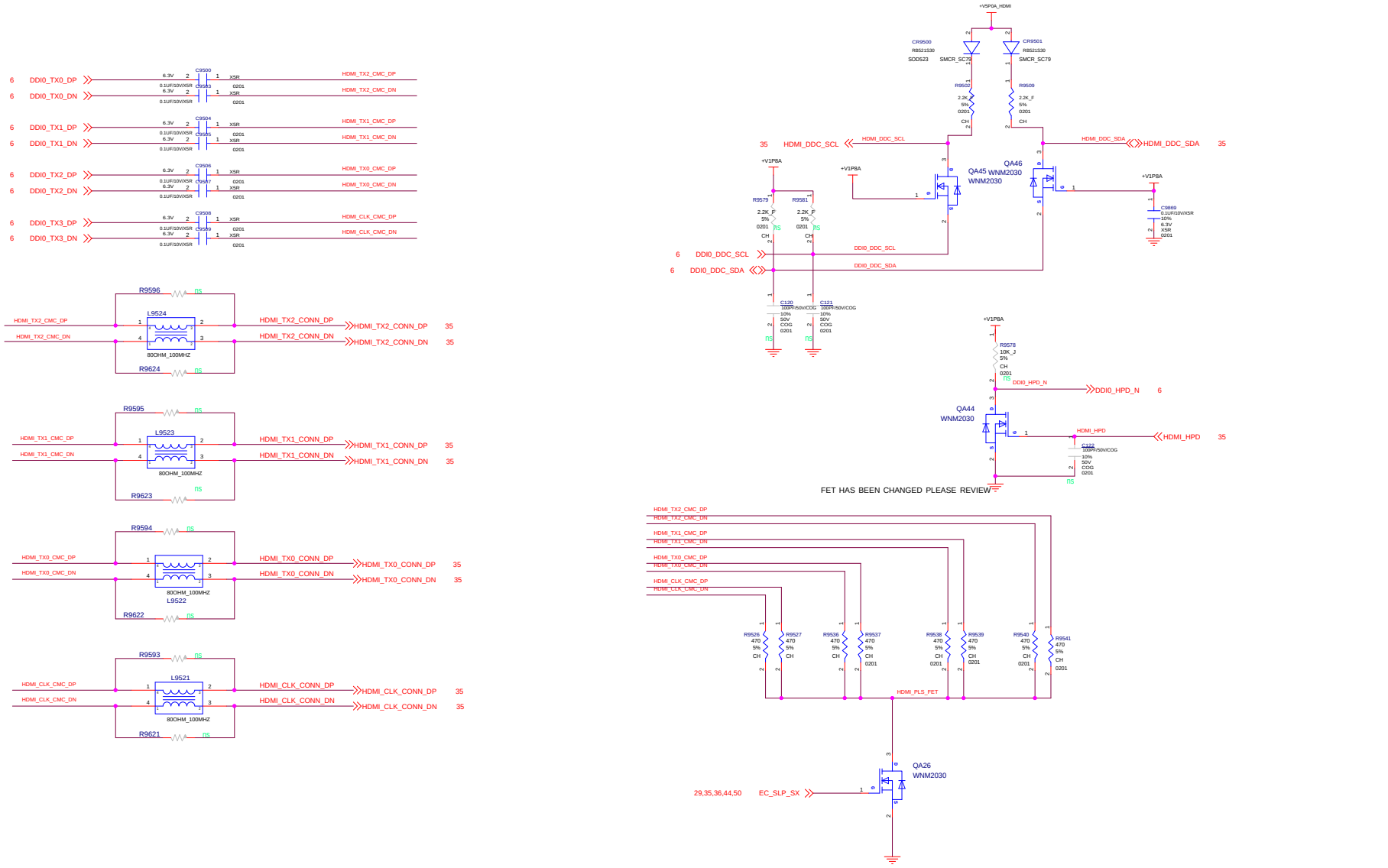
[PCH_PWROK, RSMRST_B, PROCHOT_B, IRQ_B]
These pins are open drain outputs and
need pull-up resisters according to the condition of the connected devices.



APOLLO LAKE

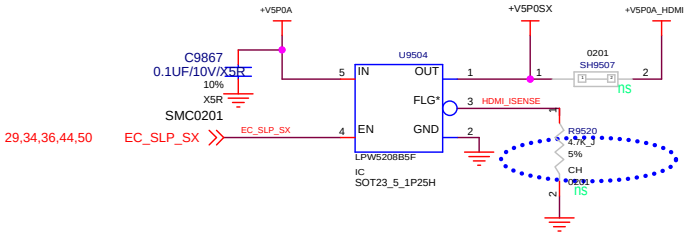
Title	APOLLO LAKE		
Size: Custom	Document Number: POWER DELIVERY1.8V AND 1.0V		Rev: R100
Date: Tuesday, December 06, 2016	Sheet 33 of 57		

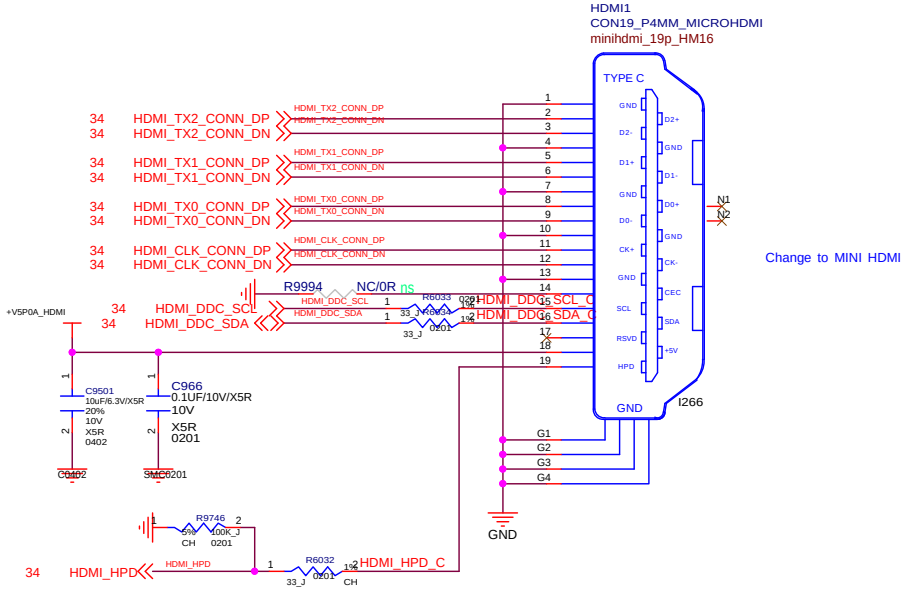
HDMI LEVEL SHIFTERS & CONNECTOR

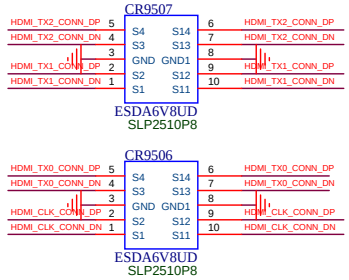


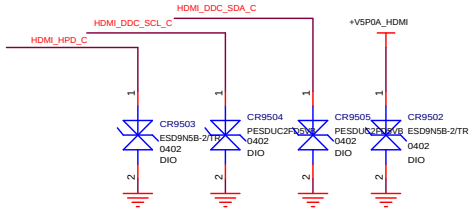
FET HAS BEEN CHANGED PLEASE REVIEW

APOLLO LAKE			
Title: APOLLO LAKE			
Size: C	Document Number: HDMI LEVEL SHIFTERS		Rev: R100
Date: Tuesday, December 06, 2016	Sheet 34 of 57		

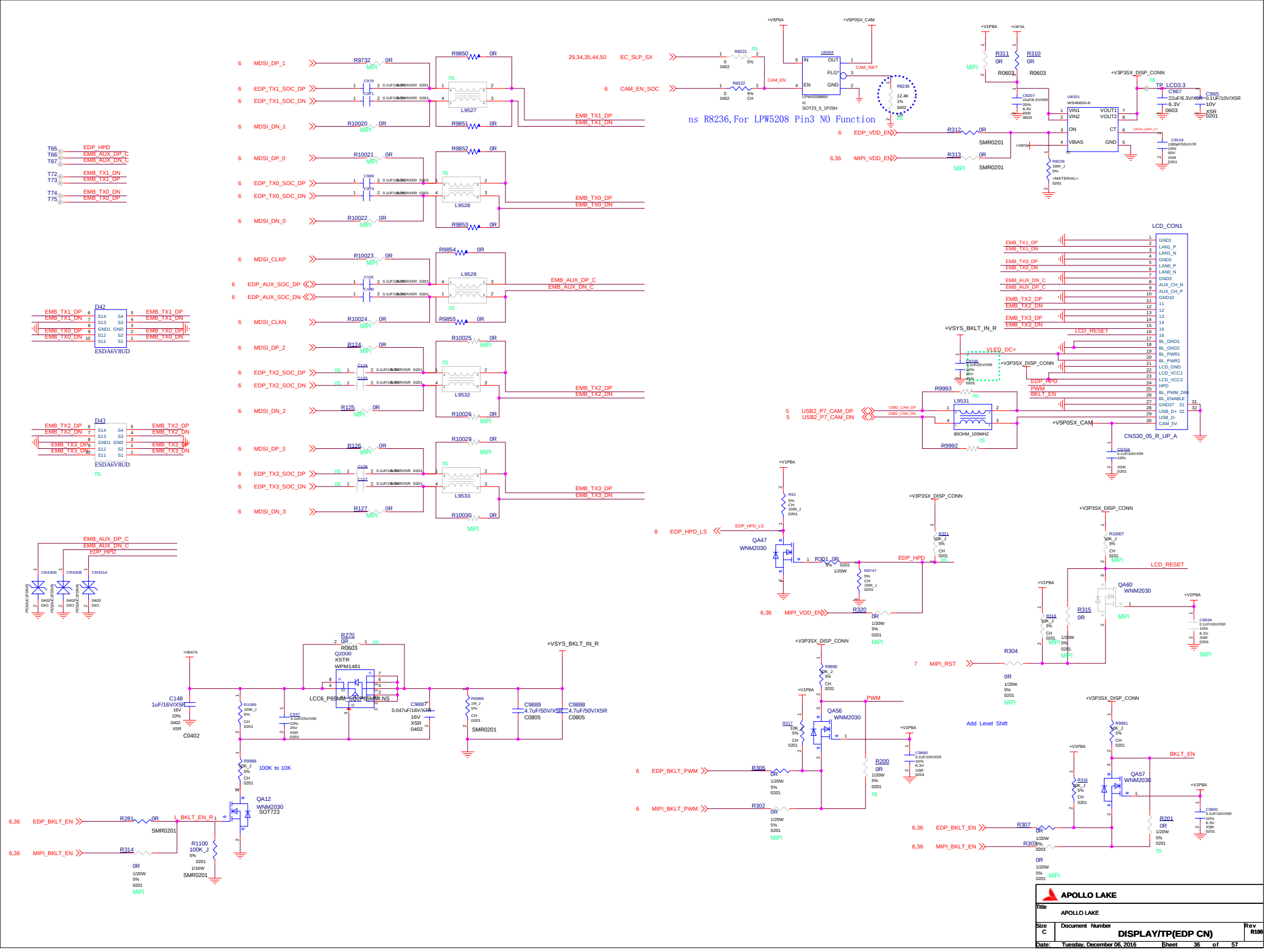


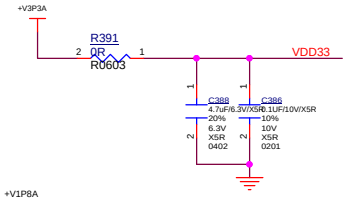


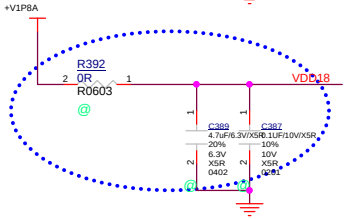




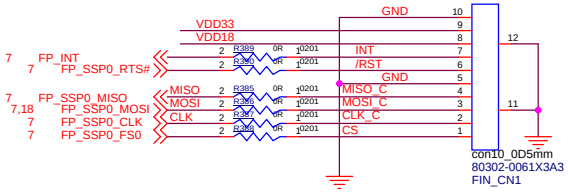
APOLLO LAKE			
Title: APOLLO LAKE			
Size: B	Document Number: HDMI CONNECTOR		Rev: R100
Date: Tuesday, December 06, 2016	Sheet 35 of 57		


MDSI_DP_1
EDP_TX1_SOC_DP
EDP_TX1_SOC_DN
MDSI_DN_1
EMB_TX1_DP
EMB_TX1_DN
MDSI_DP_0
EDP_TX0_SOC_DP
EDP_TX0_SOC_DN
MDSI_DN_0
EMB_TX0_DP
EMB_TX0_DN
MDSI_CLKP
EDP_AUX_SOC_DP
EDP_AUX_SOC_DN
MDSI_CLKN
EMB_AUX_DP_C
EMB_AUX_DN_C
MDSI_DP_2
EDP_TX2_SOC_DP
EDP_TX2_SOC_DN
MDSI_DN_2
EMB_TX2_DP
EMB_TX2_DN
MDSI_DP_3
EDP_TX3_SOC_DP
EDP_TX3_SOC_DN
MDSI_DN_3
EMB_TX3_DP
EMB_TX3_DN
EC_SLP_SX
CAM_EN_SOC
CAM_EN
CAM_ISET
ns R8236, For LPW5208 Pin3 NO Function
EDP_VDD_EN
MIPI_VDD_EN
LCD_CON1
LCD_RESET
VLED_DC+
PWM
BKLT_EN
USB2_P7_CAM_DP
USB2_P7_CAM_DN
CNS30_05_R_UP_A
EDP_HPD_LS
MIPI_VDD_EN
MIPI_RST
Add Level Shift
EDP_BKLT_PWM
MIPI_BKLT_PWM
EDP_BKLT_EN
MIPI_BKLT_EN
+VSYS_BKLT_IN_R
+VBATA
+V1P8A
+V3P3A
+V5P0A
+V5P0SX_CAM
+V3P3SX_DISP_CONN
ESDA6V8UD
APOLLO LAKE
DISPLAY/TP(EDP CN)
Tuesday, December 06, 2016
Sheet 36 of 57



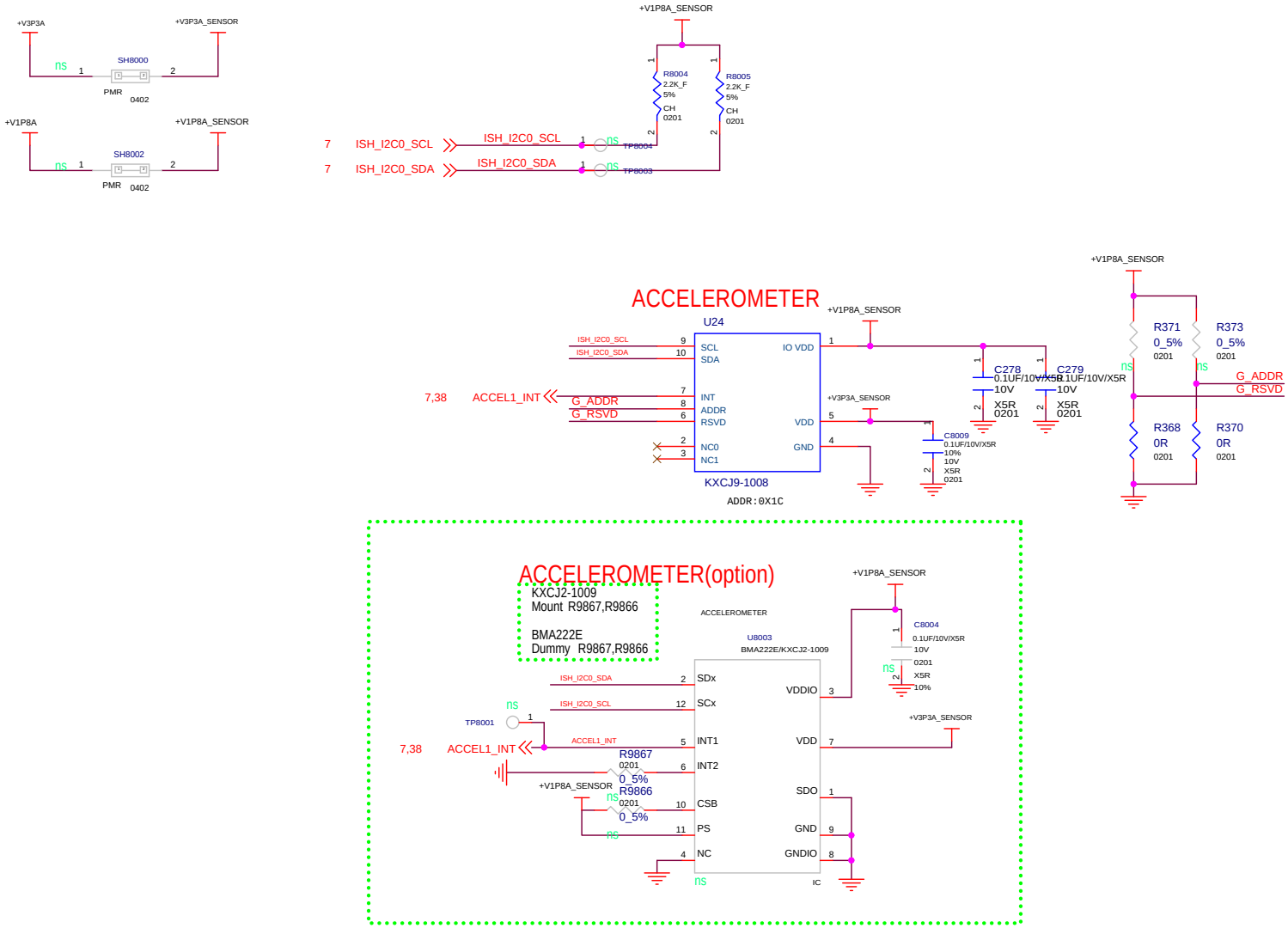


NS +V1P8A



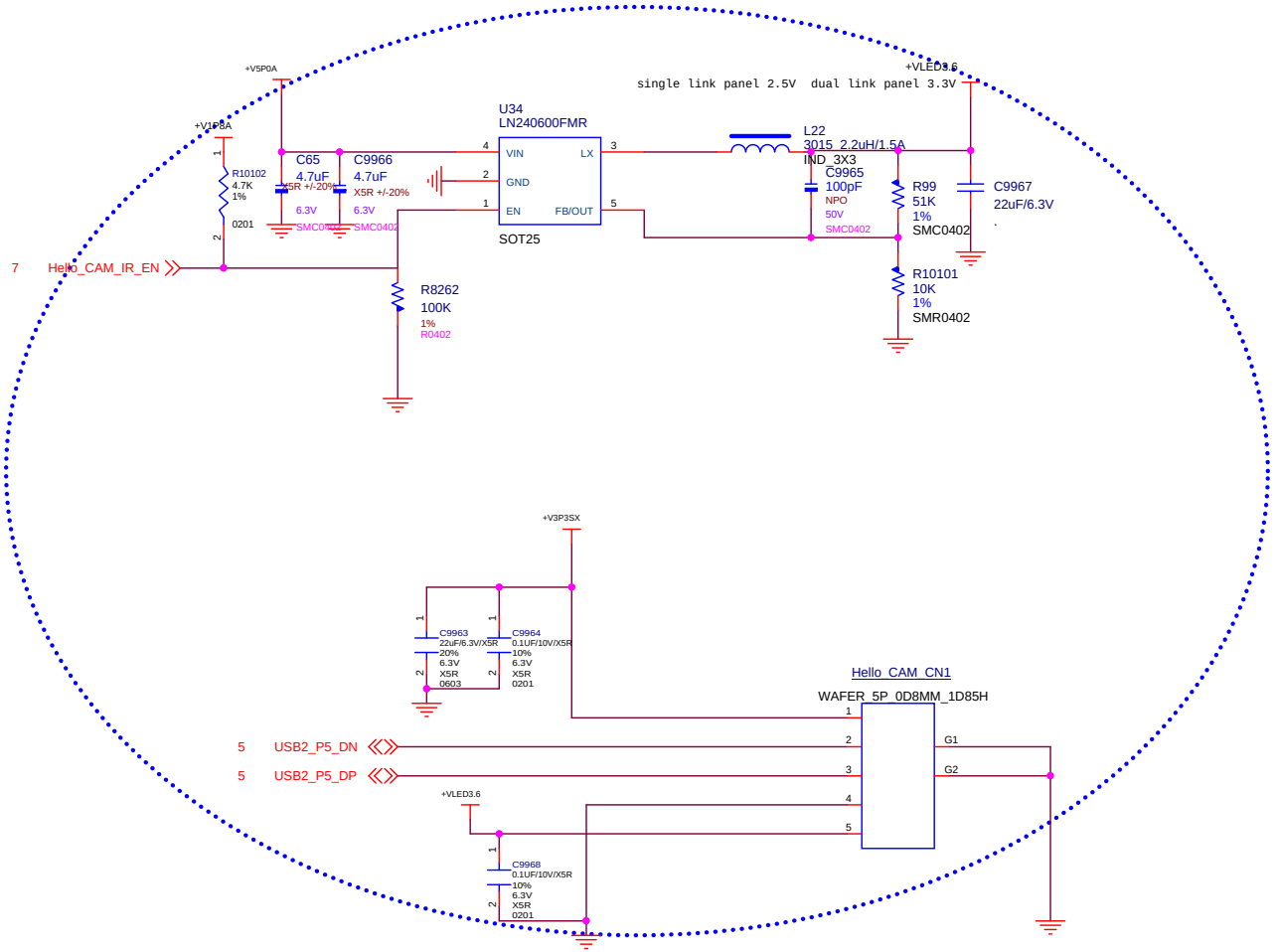
APOLLO LAKE

Title	APOLLO LAKE	
Size: Custom	Document Number: TOUCH PANEL AND DOCK	Rev: R100
Date: Tuesday, December 06, 2016	Sheet 37 of 57	



APOLLO LAKE			
Title: APOLLO LAKE			
Size: B	Document Number: SENSORS		Rev: R100
Date: Tuesday, December 06, 2016	Sheet 38 of 57		

ACCEL I2C ADDR: 0X18



R120
Add Hello CAM

APOLLO LAKE

Title	APOLLO LAKE	
Size B	Document Number FRONT AND REAR CAMERA CONN	Rev R100
Date: Friday, December 09, 2016	Sheet 39 of 57	

APOLLO LAKE

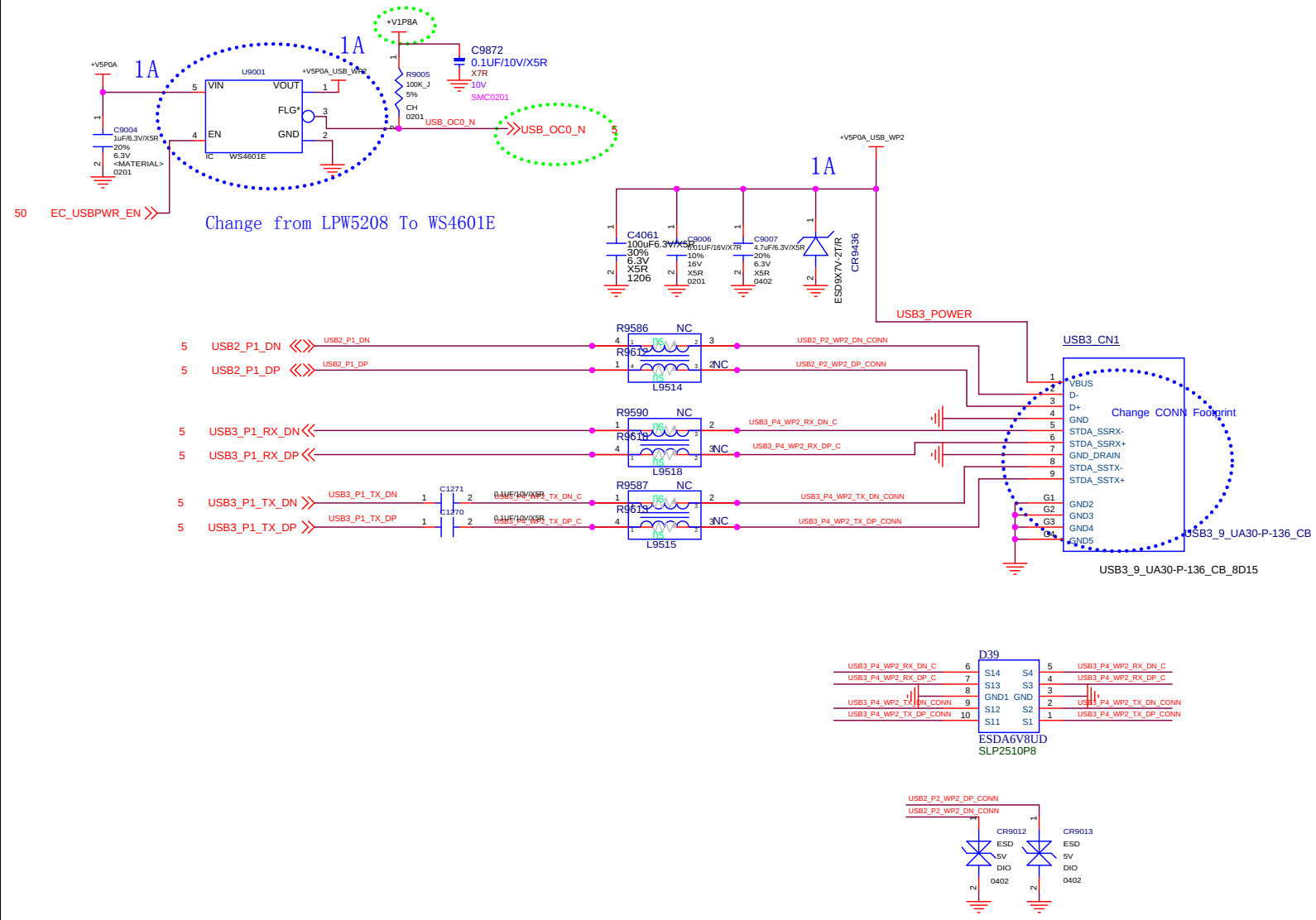
Title
APOLLO LAKE

Size	Document Number	Rev
B	CAMERA DISCRETE CNTRL LOGIC	R100

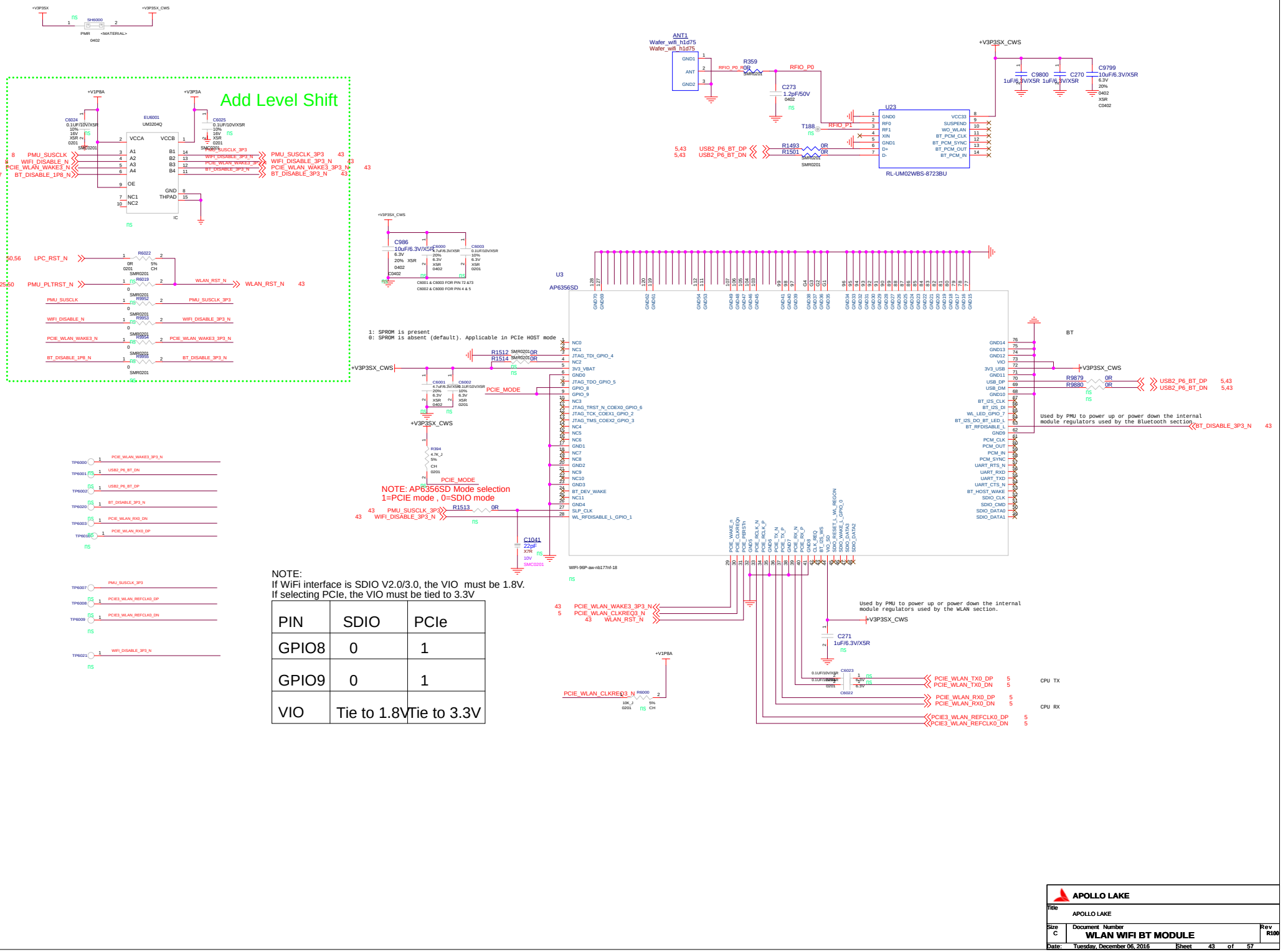
Date: Tuesday, December 06, 2016 Sheet 40 of 57

APOLLO LAKE

Title	APOLLO LAKE	
Size: Custom	Document Number: COB TP	Rev: R100
Date: Tuesday, December 06, 2016	Sheet 41 of 57	



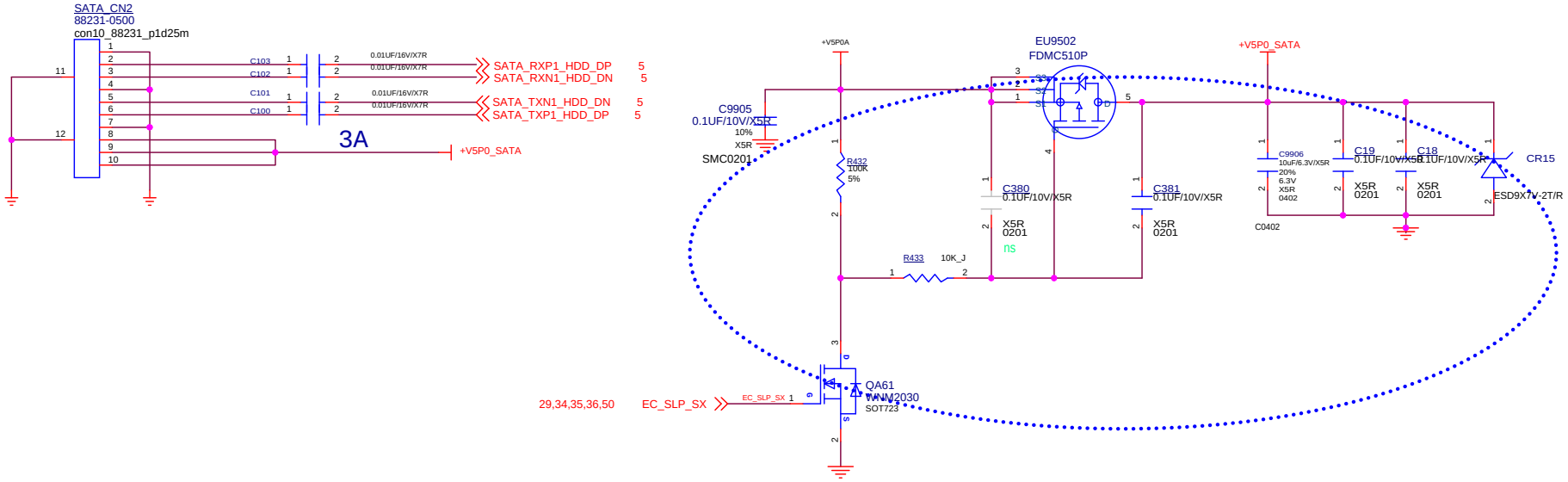
APOLLO LAKE			
Title: APOLLO LAKE			
Size: B	Document Number: USB3.0 CONN		Rev: R100
Date: Tuesday, December 06, 2016	Sheet 42 of 57		



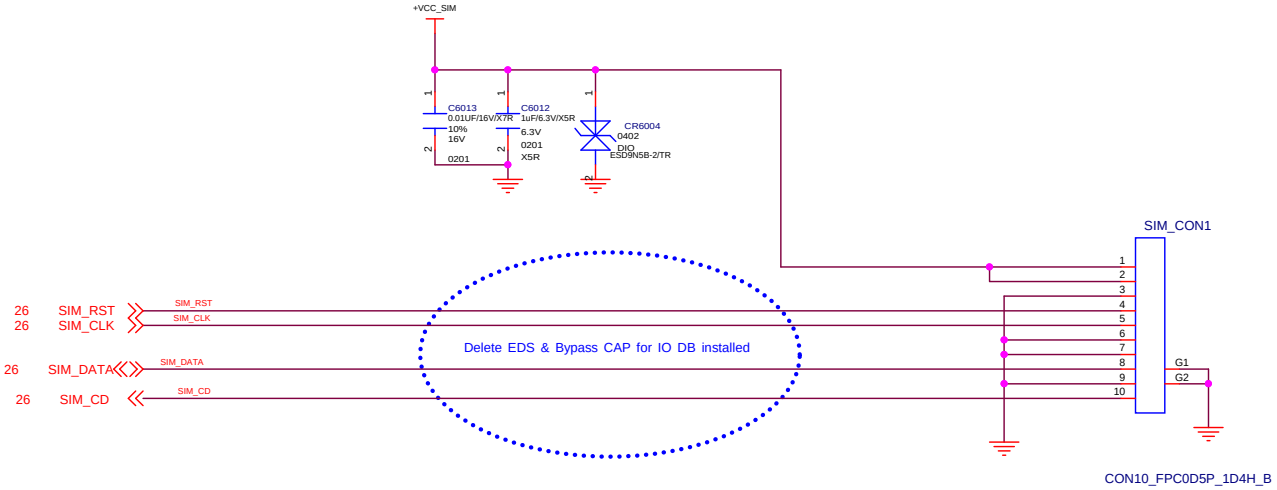
NOTE:
If WiFi interface is SDIO V2.0/3.0, the VIO must be 1.8V.
If selecting PCIe, the VIO must be tied to 3.3V

PIN	SDIO	PCIe
GPIO8	0	1
GPIO9	0	1
VIO	Tie to 1.8V	Tie to 3.3V

Title	APOLLO LAKE
Size	C
Document Number	WLAN WIFI BT MODULE
Rev	R100
Date:	Tuesday, December 06, 2016
Sheet	43 of 57

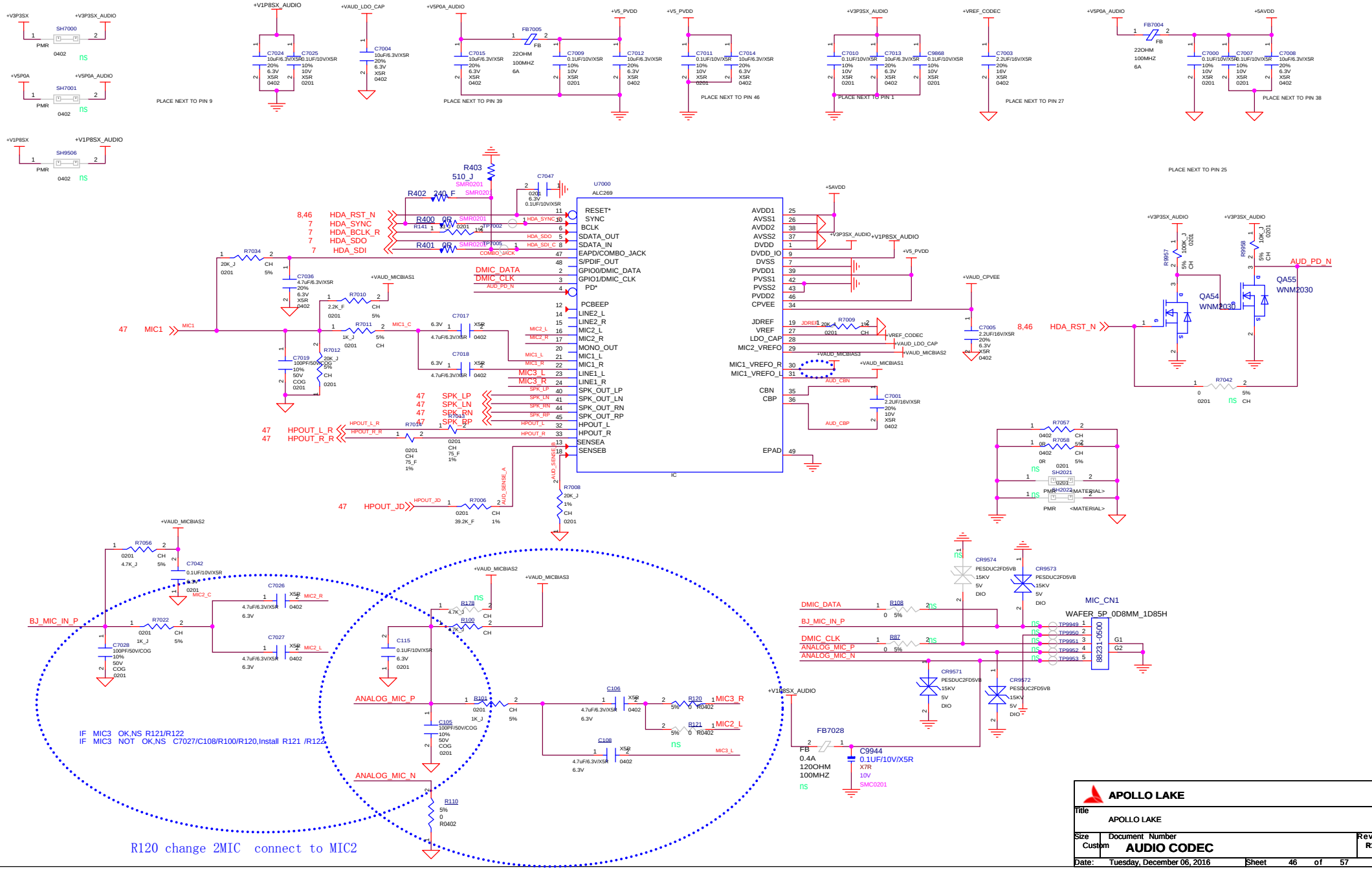


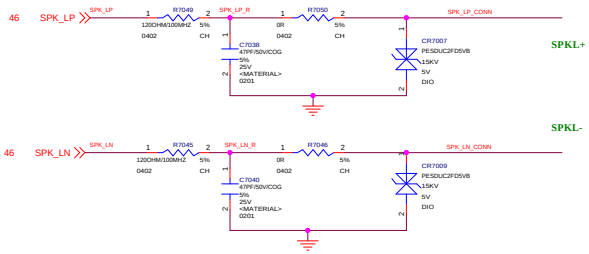
APOLLO LAKE			
Title: APOLLO LAKE			
Size: B	Document Number: WWAN MODULE		Rev: R100
Date: Tuesday, December 06, 2016	Sheet 44 of 57		

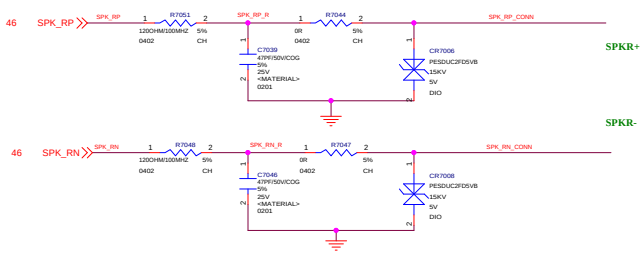


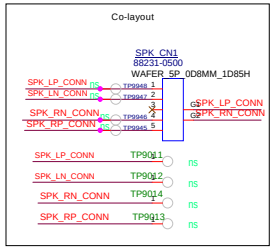
APOLLO LAKE

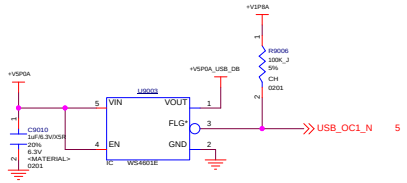
Title	APOLLO LAKE		
Size B	Document Number MICRO SIM		Rev R100
Date: Tuesday, December 06, 2016	Sheet 45 of 57		

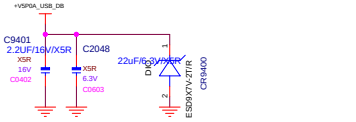

+V3P3SX
+V3P3SX_AUDIO
SH7000
PMR
0402
ns
+V5P0A
+V5P0A_AUDIO
SH7001
PMR
0402
ns
+V1P8SX
+V1P8SX_AUDIO
SH9506
PMR
0402
ns
+V1P8SX_AUDIO
C7024 10uF/6.3V/X5R 20% 6.3V X5R 0402
C7025 0.1UF/10V/X5R 10% 10V X5R 0201
PLACE NEXT TO PIN 9
+VAUD_LDO_CAP
C7004 10uF/6.3V/X5R 20% 6.3V X5R 0402
+V5P0A_AUDIO
FB7005
FB
22OHM
100MHZ
6A
C7015 10uF/6.3V/X5R 20% 6.3V X5R 0402
C7009 0.1UF/10V/X5R 10% 10V X5R 0201
C7012 10uF/6.3V/X5R 20% 6.3V X5R 0402
PLACE NEXT TO PIN 39
+V5_PVDD
C7011 0.1UF/10V/X5R 10% 10V X5R 0201
C7014 10uF/6.3V/X5R 20% 6.3V X5R 0402
PLACE NEXT TO PIN 46
+V3P3SX_AUDIO
C7010 0.1UF/10V/X5R 10% 10V X5R 0201
C7013 10uF/6.3V/X5R 20% 6.3V X5R 0402
C9868 0.1UF/10V/X5R 10% 10V X5R 0201
PLACE NEXT TO PIN 1
+VREF_CODEC
C7003 2.2UF/16V/X5R 20% 16V X5R 0402
PLACE NEXT TO PIN 27
+V5P0A_AUDIO
FB7004
FB
22OHM
100MHZ
6A
+5AVDD
C7000 0.1UF/10V/X5R 10% 10V X5R 0201
C7007 0.1UF/10V/X5R 10% 10V X5R 0201
C7008 10uF/6.3V/X5R 20% 6.3V X5R 0402
PLACE NEXT TO PIN 38
PLACE NEXT TO PIN 25
R403 510_J SMR0201
R402 240_F SMR0201
C7047 0.1UF/10V/X5R
U7000
ALC269
8,46 HDA_RST_N
7 HDA_SYNC
7 HDA_BCLK_R
7 HDA_SDO
7 HDA_SDI
R400 0R SMR0201
R401 0R SMR0201
TP7002
TP7005
COMBO_JACK
HDA_SYNC
HDA_SDO
HDA_SDI_C
RESET*
SYNC
BCLK
SDATA_OUT
SDATA_IN
EAPD/COMBO_JACK
S/PDIF_OUT
GPIO0/DMIC_DATA
GPIO1/DMIC_CLK
PD*
PCBEEP
LINE2_L
LINE2_R
MIC2_L
MIC2_R
MONO_OUT
MIC1_L
MIC1_R
LINE1_L
LINE1_R
SPK_OUT_LP
SPK_OUT_LN
SPK_OUT_RN
SPK_OUT_RP
HPOUT_L
HPOUT_R
SENSEA
SENSEB
EPAD
IC
DMIC_DATA
DMIC_CLK
AUD_PD_N
AVDD1
AVSS1
AVDD2
AVSS2
DVDD
DVDD_IO
DVSS
PVDD1
PVSS1
PVSS2
PVDD2
CPVEE
JDREF
VREF
LDO_CAP
MIC2_VREFO
MIC1_VREFO_R
MIC1_VREFO_L
CBN
CBP
R7034 20K_J 0201
C7036 4.7uF/6.3V/X5R 20% 6.3V X5R 0402
R7010 2.2K_F 0201
R7011 1K_J 0201
C7017 4.7uF/6.3V/X5R 6.3V X5R 0402
R7012 20K_J 0201
C7019 100PF/50V/COG 10% 50V COG 0201
C7018 4.7uF/6.3V/X5R 6.3V X5R 0402
MIC3_L
MIC3_R
47 MIC1
47 SPK_LP
47 SPK_LN
47 SPK_RN
47 SPK_RP
47 HPOUT_L_R
47 HPOUT_R_R
R7013 0201 CH 75_F 1%
R7014 0201 CH 75_F 1%
47 HPOUT_JD
R7006 39.2K_F 0201 CH 1%
R7008 20K_J 0201 CH 1%
R7009 20K_J 0201 CH
C7005 2.2UF/16V/X5R 20% 6.3V X5R 0402
C7001 2.2UF/16V/X5R 20% 10V X5R 0402
AUD_CBN
AUD_CBP
+VAUD_MICBIAS1
+VAUD_MICBIAS2
+VAUD_MICBIAS3
+VAUD_CPVEE
+VREF_CODEC
+VAUD_LDO_CAP
8,46 HDA_RST_N
AUD_PD_N
QA54 WNM2030
QA55 WNM2030
R9957 100K_J 0201
R9958 10K_J 0201
R7042 0 0201
R7057 0R 0402
R7058 0R 0402
SH2021
PMR
<MATERIAL>
+VAUD_MICBIAS2
R7056 4.7K_J 0201
C7042 0.1UF/10V/X5R
BJ_MIC_IN_P
R7022 1K_J 0201
C7028 100PF/50V/COG 10% 50V COG 0201
C7026 4.7uF/6.3V/X5R 6.3V 0402
C7027 4.7uF/6.3V/X5R 6.3V 0402
MIC2_C
MIC2_R
MIC2_L
IF MIC3 OK,NS R121/R122
IF MIC3 NOT OK,NS C7027/C108/R100/R120,Install R121 /R122
ANALOG_MIC_P
ANALOG_MIC_N
R178 4.7K_J
R100 4.7K_J
C115 0.1UF/10V/X5R 6.3V 0201
R101 1K_J 0201
C105 100PF/50V/COG 10% 50V COG 0201
C106 4.7uF/6.3V/X5R 6.3V 0402
C108 4.7uF/6.3V/X5R 6.3V 0402
R120 0 0402
R121 0 0402
R110 0 0402
R120 change 2MIC connect to MIC2
CR9574 PESDUC2FD5VB 15KV 5V DIO
CR9573 PESDUC2FD5VB 15KV 5V DIO
CR9571 PESDUC2FD5VB 15KV 5V DIO
CR9572 PESDUC2FD5VB 15KV 5V DIO
MIC_CN1
WAFER_5P_0D8MM_1D85H
88231-0500
TP9949
TP9950
TP9951
TP9952
TP9953
G1
G2
R108 0 5%
R87 0 5%
FB7028
FB 0.4A 120OHM 100MHZ
C9944 0.1UF/10V/X5R X7R 10V SMC0201
APOLLO LAKE
Title
APOLLO LAKE
Size Custom
Document Number
AUDIO CODEC
Rev R100
Date: Tuesday, December 06, 2016
Sheet 46 of 57

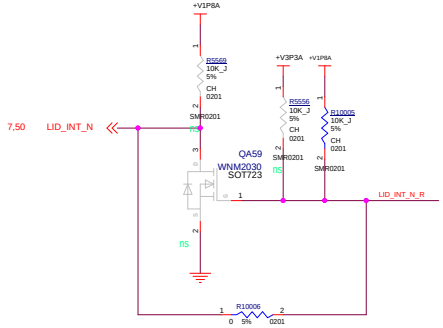


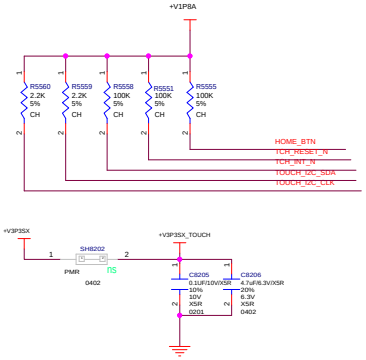


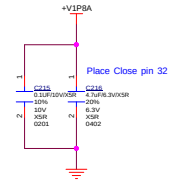


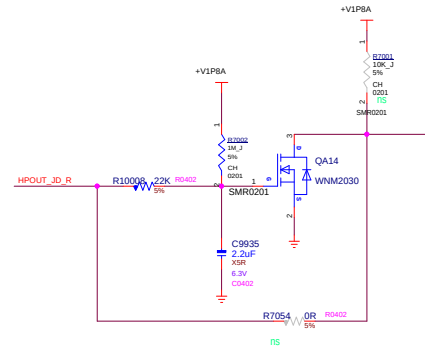


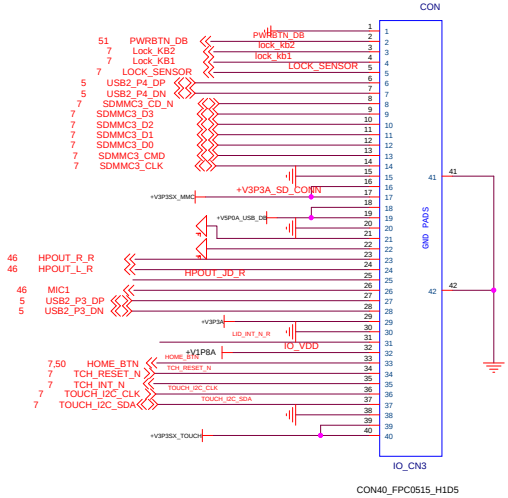






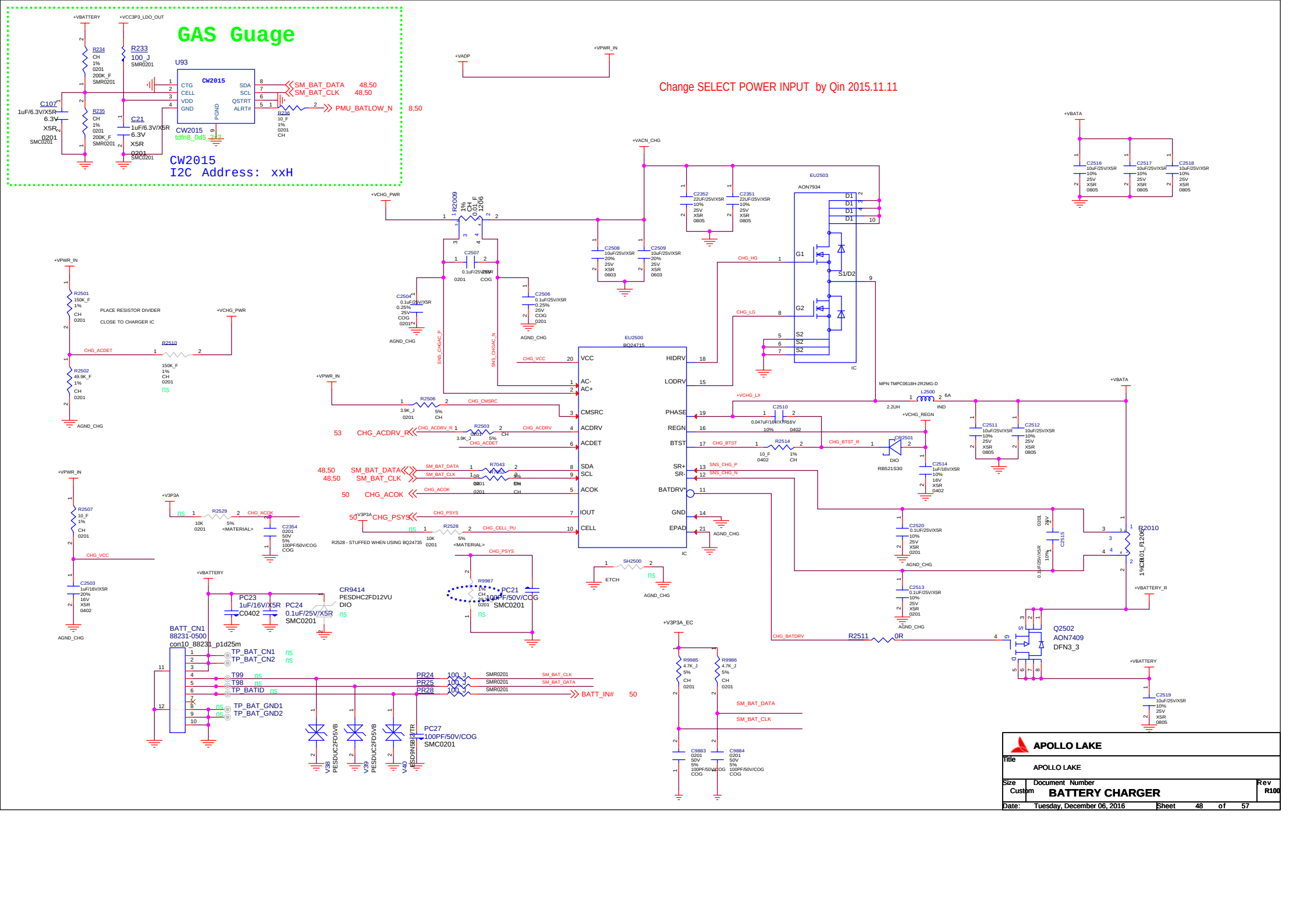






APOLLO LAKE

Title	APOLLO LAKE	
Size C	Document Number AUDIO-HEADSET AND SPKRS	Rev R100
Date: Tuesday, December 06, 2016	Sheet 47 of 57	


GAS Guage
U93
CW2015
CTG
CELL
VDD
GND
SDA
SCL
QSTRT
ALRT#
PGND
SM_BAT_DATA 48,50
SM_BAT_CLK 48,50
PMU_BATLOW_N 8,50
CW2015
I2C Address: xxH
Change SELECT POWER INPUT by Qin 2015.11.11
EU2500
BQ24715
EU2503
AON7934
PLACE RESISTOR DIVIDER
CLOSE TO CHARGER IC
CHG_ACDRV_R 53
CHG_ACOK 50
CHG_PSYS 50
SM_BAT_DATA 48,50
SM_BAT_CLK 48,50
BATT_IN# 50
R2528 - STUFFED WHEN USING BQ24735
BATT_CN1
88231-0500
con10_88231_p1d25m
CR9414
PESDHC2FD12VU
DIO
PC23
1uF/16V/X5R
C0402
PC24
0.1uF/25V/X5R
SMC0201
PC21
100PF/50V/COG
SMC0201
PC27
100PF/50V/COG
SMC0201
Q2502
AON7409
DFN3_3
R2511 0R
MPN:TMPC0618H-2R2MG-D
L2500
2.2UH
IND
6A
CB2501
RB521S30
DIO
APOLLO LAKE
Title
APOLLO LAKE
Size
Custom
Document Number
BATTERY CHARGER
Rev
R100
Date: Tuesday, December 06, 2016
Sheet 48 of 57

APOLLO LAKE

Title
APOLLO LAKE

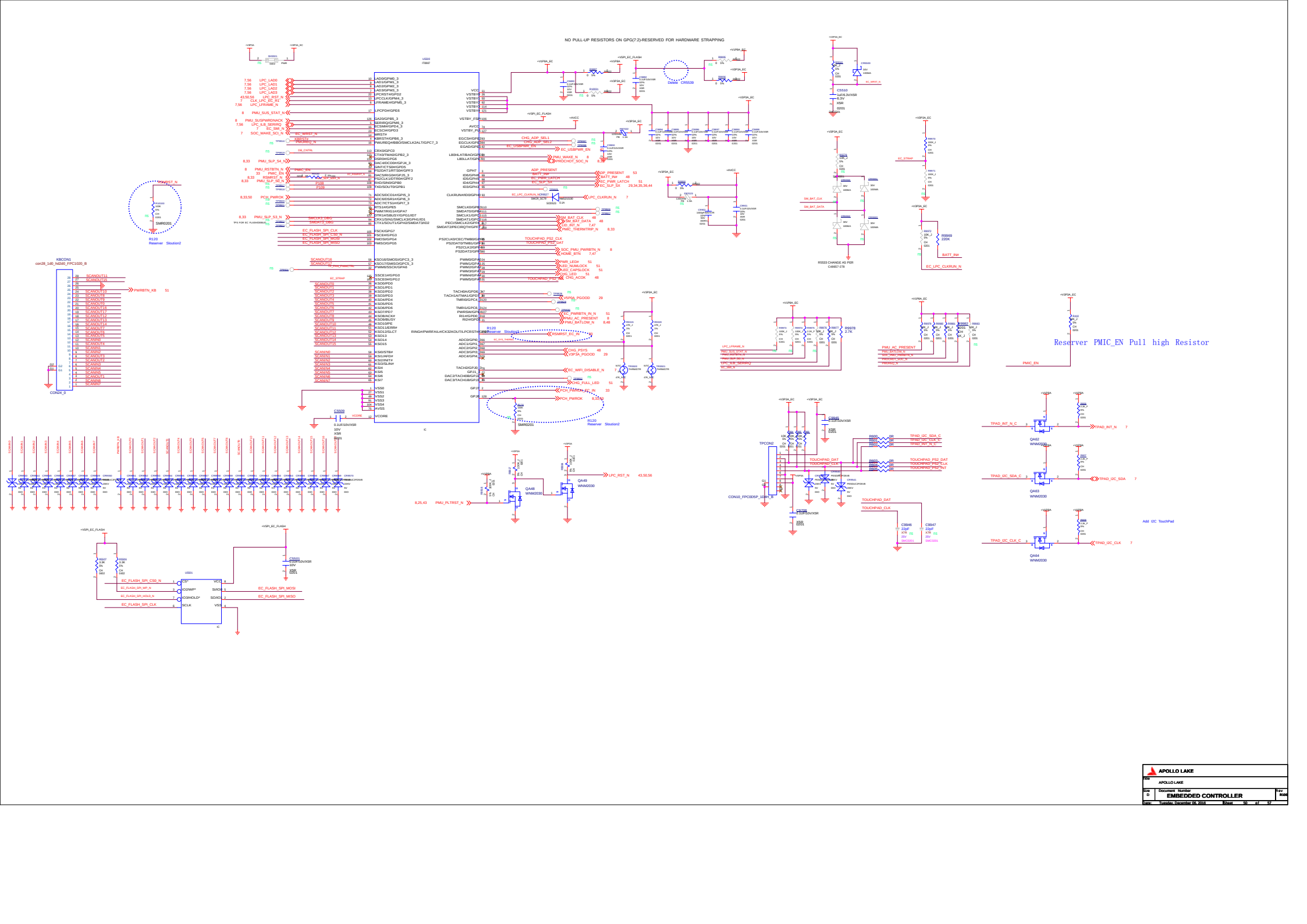
Size
B

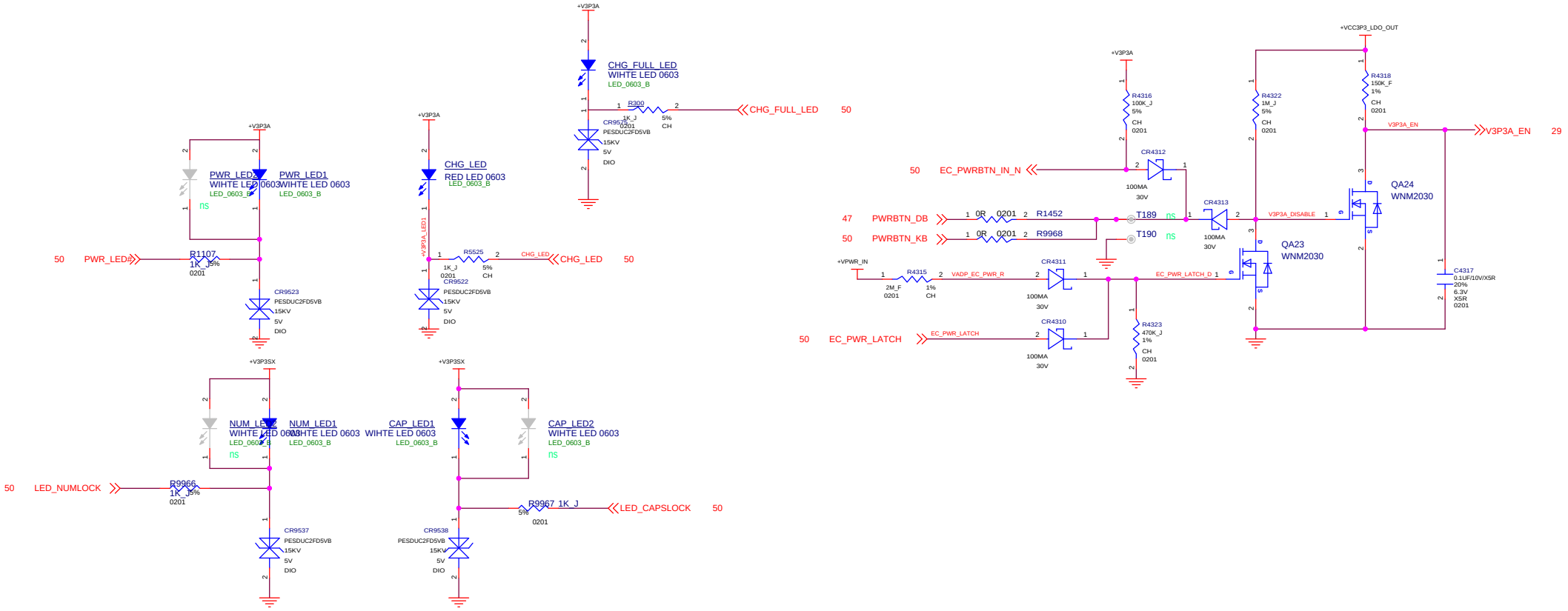
Document Number
DC JACK

Rev
R100

Date: Tuesday, December 06, 2016

Sheet 49 of 57


NO PULL-UP RESISTORS ON GPG(7:2)-RESERVED FOR HARDWARE STRAPPING
Reserver PMIC_EN Pull high Resistor
Add I2C TouchPad
APOLLO LAKE
EMBEDDED CONTROLLER
Tuesday, December 06, 2016

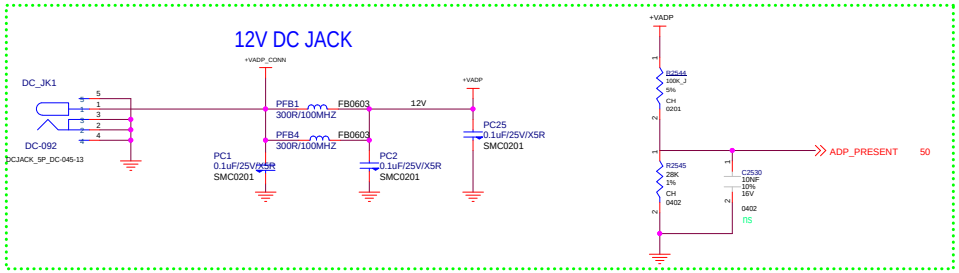


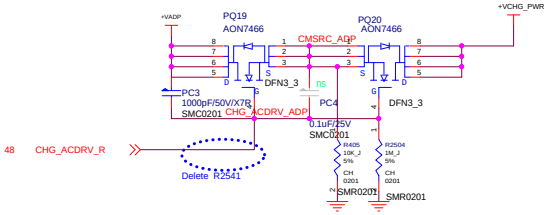
APOLLO LAKE

Title	APOLLO LAKE	
Size: Custom	Document Number: BUTTONS LEDS AND MISC	Rev: R100
Date: Tuesday, December 06, 2016	Sheet 51 of 57	

APOLLO LAKE

Title	APOLLO LAKE	
Size: Custom	Document Number: TYPE-C MULTIPLEXER	Rev: R100
Date: Tuesday, December 06, 2016	Sheet 52 of 57	





APOLLO LAKE

Title	APOLLO LAKE	
Size C	Document Number TYPE-C PD CONTROLLER	Rev R100
Date: Tuesday, December 06, 2016	Sheet 53 of 57	

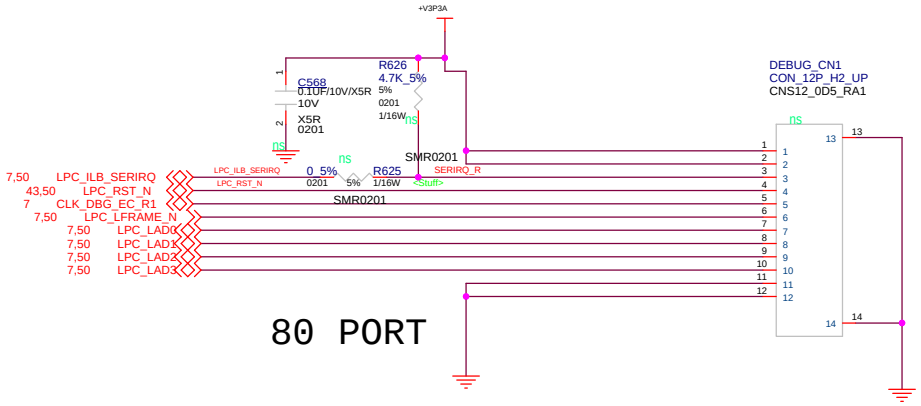
BLANK

APOLLO LAKE		
Title: APOLLO LAKE		
Size: Custom	Document Number: XX	Rev: R100
Date: Tuesday, December 06, 2016	Sheet 54 of 57	

BLANK

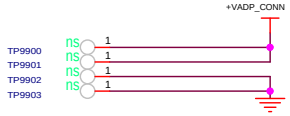
APOLLO LAKE

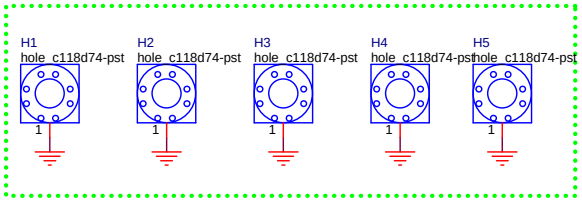
Title: APOLLO LAKE		
Size: Custom	Document Number: TYPE-C CONNECTOR	Rev: R100
Date: Tuesday, December 06, 2016	Sheet 55 of 57	



APOLLO LAKE

Title	APOLLO LAKE	
Size: Custom	Document Number: DEBUG	Rev: R100
Date: Tuesday, December 06, 2016	Sheet 56 of 57	

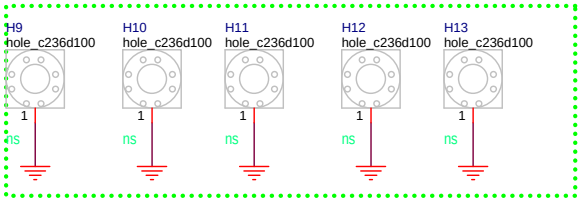




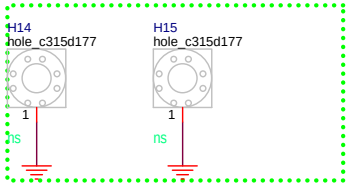
For Themal

MTG_PLATED_THRU
HT1
ns

MTG_PLATED_THRU
HT2
ns



For ME



For ME

APOLLO LAKE			
Title: APOLLO LAKE			
Size: B	Document Number: FACTORY TEST POINTS		Rev: R100
Date: Tuesday, December 06, 2016	Sheet 57 of 57		