


APOLLO LAKE

Y116AR100

LPDDR3 216 Ball x2

 APOLLO LAKE		
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20,22	LPDDR3_CH1_CAB7	LPDDR3_CH1_CAB7	BG9	DDR3L_CH1_MA0 / LPDDR3_CH1_CAB7	DDR3L_CH1_D00 / LPDDR3_CH1_D0A0	BJ26	LPDDR3_CH1_D0A0	LPDDR3_CH1_D0A0	20
20,22	LPDDR3_CH1_CAB8	LPDDR3_CH1_CAB8	BG10	DDR3L_CH1_MA1 / LPDDR3_CH1_CAB8	DDR3L_CH1_D01 / LPDDR3_CH1_D0A1	BG30	LPDDR3_CH1_D0A1	LPDDR3_CH1_D0A1	20
20,22	LPDDR3_CH1_CAB5	LPDDR3_CH1_CAB5	BH9	DDR3L_CH1_MA2 / LPDDR3_CH1_CAB5	DDR3L_CH1_D02 / LPDDR3_CH1_D0A2	BH31	LPDDR3_CH1_D0A2	LPDDR3_CH1_D0A2	20
			B016	DDR3L_CH1_MA3 / LPDDR3_CH1_NC	DDR3L_CH1_D03 / LPDDR3_CH1_D0A3	BG31	LPDDR3_CH1_D0A3	LPDDR3_CH1_D0A3	20
			BH16	DDR3L_CH1_MA4 / LPDDR3_CH1_NC	DDR3L_CH1_D04 / LPDDR3_CH1_D0A4	BH27	LPDDR3_CH1_D0A4	LPDDR3_CH1_D0A4	20
			BG13	DDR3L_CH1_MA5 / LPDDR3_CH1_CAA2	DDR3L_CH1_D05 / LPDDR3_CH1_D0A5	BG27	LPDDR3_CH1_D0A5	LPDDR3_CH1_D0A5	20
20,22	LPDDR3_CH1_CAA2	LPDDR3_CH1_CAA2	B112	DDR3L_CH1_MA6 / LPDDR3_CH1_CAA0	DDR3L_CH1_D06 / LPDDR3_CH1_D0A6	BG26	LPDDR3_CH1_D0A6	LPDDR3_CH1_D0A6	20
20,22	LPDDR3_CH1_CAA0	LPDDR3_CH1_CAA0	BG14	DDR3L_CH1_MA7 / LPDDR3_CH1_CAA3	DDR3L_CH1_D07 / LPDDR3_CH1_D0A7	BJ30	LPDDR3_CH1_D0A7	LPDDR3_CH1_D0A7	20
20,22	LPDDR3_CH1_CAA3	LPDDR3_CH1_CAA3	BG12	DDR3L_CH1_MA8 / LPDDR3_CH1_CAA1	DDR3L_CH1_D08 / LPDDR3_CH1_D0A8	BA30	LPDDR3_CH1_D0A8	LPDDR3_CH1_D0A8	20
20,22	LPDDR3_CH1_CAA1	LPDDR3_CH1_CAA1	BH11	DDR3L_CH1_MA9 / LPDDR3_CH1_CAA4	DDR3L_CH1_D09 / LPDDR3_CH1_D0A9	B830	LPDDR3_CH1_D0A9	LPDDR3_CH1_D0A9	20
20,22	LPDDR3_CH1_CAB6	LPDDR3_CH1_CAB6	BG7	DDR3L_CH1_MA10 / LPDDR3_CH1_CAB6	DDR3L_CH1_D010 / LPDDR3_CH1_D0A10	B830	LPDDR3_CH1_D0A10	LPDDR3_CH1_D0A10	20
20,22	LPDDR3_CH1_CAB6	LPDDR3_CH1_CAB6	BH13	DDR3L_CH1_MA11 / LPDDR3_CH1_CAA6	DDR3L_CH1_D011 / LPDDR3_CH1_D0A11	B230	LPDDR3_CH1_D0A11	LPDDR3_CH1_D0A11	20
20,22	LPDDR3_CH1_CAA6	LPDDR3_CH1_CAA6	BG13	DDR3L_CH1_MA12 / LPDDR3_CH1_CAA5	DDR3L_CH1_D012 / LPDDR3_CH1_D0A12	BE25	LPDDR3_CH1_D0A12	LPDDR3_CH1_D0A12	20
20,22	LPDDR3_CH1_CAA5	LPDDR3_CH1_CAA5	BH3	DDR3L_CH1_MA13 / LPDDR3_CH1_CAB0	DDR3L_CH1_D013 / LPDDR3_CH1_D0A13	B827	LPDDR3_CH1_D0A13	LPDDR3_CH1_D0A13	20
20,22	LPDDR3_CH1_CAB8	LPDDR3_CH1_CAB8	BG15	DDR3L_CH1_MA14 / LPDDR3_CH1_CAA8	DDR3L_CH1_D014 / LPDDR3_CH1_D0A14	BD25	LPDDR3_CH1_D0A14	LPDDR3_CH1_D0A14	20
20,22	LPDDR3_CH1_CAA9	LPDDR3_CH1_CAA9	BG16	DDR3L_CH1_MA15 / LPDDR3_CH1_CAA9	DDR3L_CH1_D015 / LPDDR3_CH1_D0A15	BD27	LPDDR3_CH1_D0A15	LPDDR3_CH1_D0A15	20
			BG24	DDR3L_CH1_D016 / LPDDR3_CH1_D0A16	DDR3L_CH1_D016 / LPDDR3_CH1_D0A16	BG24	LPDDR3_CH1_D0A16	LPDDR3_CH1_D0A16	20
20,22	LPDDR3_CH1_CAB2	LPDDR3_CH1_CAB2	BH6	DDR3L_CH1_BA0 / LPDDR3_CH1_CAB2	DDR3L_CH1_D018 / LPDDR3_CH1_D0A18	BH23	LPDDR3_CH1_D0A18	LPDDR3_CH1_D0A18	20
20,22	LPDDR3_CH1_CAB8	LPDDR3_CH1_CAB8	BG8	DDR3L_CH1_BA1 / LPDDR3_CH1_CAB8	DDR3L_CH1_D019 / LPDDR3_CH1_D0A19	BJ24	LPDDR3_CH1_D0A19	LPDDR3_CH1_D0A19	20
20,22	LPDDR3_CH1_CAA7	LPDDR3_CH1_CAA7	BH15	DDR3L_CH1_BA2 / LPDDR3_CH1_CAA7	DDR3L_CH1_D020 / LPDDR3_CH1_D0A20	BG20	LPDDR3_CH1_D0A20	LPDDR3_CH1_D0A20	20
			BJ6	DDR3L_CH1_RASN / LPDDR3_CH1_CAB3	DDR3L_CH1_D021 / LPDDR3_CH1_D0A21	BG21	LPDDR3_CH1_D0A21	LPDDR3_CH1_D0A21	20
20,22	LPDDR3_CH1_CAB3	LPDDR3_CH1_CAB3	BH4	DDR3L_CH1_CASN / LPDDR3_CH1_CAB1	DDR3L_CH1_D022 / LPDDR3_CH1_D0A22	BH19	LPDDR3_CH1_D0A22	LPDDR3_CH1_D0A22	20
20,22	LPDDR3_CH1_CAB1	LPDDR3_CH1_CAB1	BH7	DDR3L_CH1_WEN / LPDDR3_CH1_CAB4	DDR3L_CH1_D023 / LPDDR3_CH1_D0A23	BG25	LPDDR3_CH1_D0A23	LPDDR3_CH1_D0A23	20
20,22	LPDDR3_CH1_CAB4	LPDDR3_CH1_CAB4			DDR3L_CH1_D024 / LPDDR3_CH1_D0A24	AT27	LPDDR3_CH1_D0A24	LPDDR3_CH1_D0A24	20
20	LPDDR3_CH1_CSB1_N	LPDDR3_CH1_CSB1_N	AW17	DDR3L_CH1_CS1N / LPDDR3_CH1_CSB1B	DDR3L_CH1_D025 / LPDDR3_CH1_D0A25	AW29	LPDDR3_CH1_D0A25	LPDDR3_CH1_D0A25	20
20	LPDDR3_CH1_CSB0_N	LPDDR3_CH1_CSB0_N	AW17	DDR3L_CH1_NC / LPDDR3_CH1_CSB0B	DDR3L_CH1_D026 / LPDDR3_CH1_D0A26	AR27	LPDDR3_CH1_D0A26	LPDDR3_CH1_D0A26	20
20	LPDDR3_CH1_CSA1_N	LPDDR3_CH1_CSA1_N	BH17	DDR3L_CH1_NC / LPDDR3_CH1_CSB1A	DDR3L_CH1_D027 / LPDDR3_CH1_D0A27	AT23	LPDDR3_CH1_D0A27	LPDDR3_CH1_D0A27	20
20	LPDDR3_CH1_CSA0_N	LPDDR3_CH1_CSA0_N	BD17	DDR3L_CH1_CSB0 / LPDDR3_CH1_CSB0A	DDR3L_CH1_D028 / LPDDR3_CH1_D0A28	AV27	LPDDR3_CH1_D0A28	LPDDR3_CH1_D0A28	20
			BG18	DDR3L_CH1_CKE0 / LPDDR3_CH1_CKE0A	DDR3L_CH1_D029 / LPDDR3_CH1_D0A29	AK25	LPDDR3_CH1_D0A29	LPDDR3_CH1_D0A29	20
20	LPDDR3_CH1_CKEA0_N	LPDDR3_CH1_CKEA0_N	BG17	DDR3L_CH1_CKE1 / LPDDR3_CH1_CKE1A	DDR3L_CH1_D030 / LPDDR3_CH1_D0A30	AR23	LPDDR3_CH1_D0A30	LPDDR3_CH1_D0A30	20
20	LPDDR3_CH1_CKEA1_N	LPDDR3_CH1_CKEA1_N	BH17	DDR3L_CH1_NC / LPDDR3_CH1_CKE0B	DDR3L_CH1_D031 / LPDDR3_CH1_D0A31	AW27	LPDDR3_CH1_D0A31	LPDDR3_CH1_D0A31	20
20	LPDDR3_CH1_CKEB1_N	LPDDR3_CH1_CKEB1_N	B116	DDR3L_CH1_NC / LPDDR3_CH1_CKE1B	DDR3L_CH1_D032 / LPDDR3_CH1_D0B0	BF6	LPDDR3_CH1_D0B0	LPDDR3_CH1_D0B0	20
			AW16	DDR3L_CH1_ODT0 / LPDDR3_CH1_ODTA	DDR3L_CH1_D033 / LPDDR3_CH1_D0B1	BD10	LPDDR3_CH1_D0B1	LPDDR3_CH1_D0B1	20
20	LPDDR3_CH1_ODT_A	LPDDR3_CH1_ODT_A	AV16	DDR3L_CH1_ODT1 / LPDDR3_CH1_ODTB	DDR3L_CH1_D034 / LPDDR3_CH1_D0B2	BE14	LPDDR3_CH1_D0B2	LPDDR3_CH1_D0B2	20
20	LPDDR3_CH1_ODT_B	LPDDR3_CH1_ODT_B			DDR3L_CH1_D035 / LPDDR3_CH1_D0B3	B810	LPDDR3_CH1_D0B3	LPDDR3_CH1_D0B3	20
					DDR3L_CH1_D036 / LPDDR3_CH1_D0B4	BA14	LPDDR3_CH1_D0B4	LPDDR3_CH1_D0B4	20
					DDR3L_CH1_D037 / LPDDR3_CH1_D0B5	BB14	LPDDR3_CH1_D0B5	LPDDR3_CH1_D0B5	20
					DDR3L_CH1_D038 / LPDDR3_CH1_D0B6	BD14	LPDDR3_CH1_D0B6	LPDDR3_CH1_D0B6	20
					DDR3L_CH1_D039 / LPDDR3_CH1_D0B7	BE8	LPDDR3_CH1_D0B7	LPDDR3_CH1_D0B7	20
20	+VREFDQ1_SOC	+VREFDQ1_SOC	AT30	DDR3L_CH1_VREFDQ / LPDDR3_CH1_VREFDQ	DDR3L_CH1_D040 / LPDDR3_CH1_D0B8	AV12	LPDDR3_CH1_D0B8	LPDDR3_CH1_D0B8	20
20	+VREFCA1_SOC	+VREFCA1_SOC	AR29	DDR3L_CH1_VREFCA / LPDDR3_CH1_VREFCA	DDR3L_CH1_D041 / LPDDR3_CH1_D0B9	BG6	LPDDR3_CH1_D0B9	LPDDR3_CH1_D0B9	20
					DDR3L_CH1_D042 / LPDDR3_CH1_D0B10	BD5	LPDDR3_CH1_D0B10	LPDDR3_CH1_D0B10	20
					DDR3L_CH1_D043 / LPDDR3_CH1_D0B11	BB7	LPDDR3_CH1_D0B11	LPDDR3_CH1_D0B11	20
					DDR3L_CH1_D044 / LPDDR3_CH1_D0B12	AV10	LPDDR3_CH1_D0B12	LPDDR3_CH1_D0B12	20
20,22	LPDDR3_CH1_CLKB_N	LPDDR3_CH1_CLKB_N	BE19	DDR3L_CH1_CK0N / LPDDR3_CH1_CKN0B	DDR3L_CH1_D045 / LPDDR3_CH1_D0B13	AY9	LPDDR3_CH1_D0B13	LPDDR3_CH1_D0B13	20
20,22	LPDDR3_CH1_CLKB_P	LPDDR3_CH1_CLKB_P	BD19	DDR3L_CH1_CK0P / LPDDR3_CH1_CKP0B	DDR3L_CH1_D046 / LPDDR3_CH1_D0B14	AY7	LPDDR3_CH1_D0B14	LPDDR3_CH1_D0B14	20
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20,22	LPDDR3_CH1_CLKA_P	LPDDR3_CH1_CLKA_P	BB21	DDR3L_CH1_CKP1 / LPDDR3_CH1_CKP1A	DDR3L_CH1_D049 / LPDDR3_CH1_D0B17	AT10	LPDDR3_CH1_D0B17	LPDDR3_CH1_D0B17	20
					DDR3L_CH1_D050 / LPDDR3_CH1_D0B18	AT9	LPDDR3_CH1_D0B18	LPDDR3_CH1_D0B18	20
					DDR3L_CH1_D051 / LPDDR3_CH1_D0B19	AU1	LPDDR3_CH1_D0B19	LPDDR3_CH1_D0B19	20
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					DDR3L_CH1_D063 / LPDDR3_CH1_D0B31	BG2	LPDDR3_CH1_D0B31	LPDDR3_CH1_D0B31	20
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					DDR3L_CH1_D0S3 / LPDDR3_CH1_D0SPA3	B829	LPDDR3_CH1_D0SPA3	LPDDR3_CH1_D0SPA3	20
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					DDR3L_CH1_D0S9 / LPDDR3_CH1_D0SPA9	BD12	LPDDR3_CH1_D0SPA9	LPDDR3_CH1_D0SPA9	20
					DDR3L_CH1_D0S10 / LPDDR3_CH1_D0SPA10	B85	LPDDR3_CH1_D0SPA10	LPDDR3_CH1_D0SPA10	20
					DDR3L_CH1_D0S11 / LPDDR3_CH1_D0SPA11	B86	LPDDR3_CH1_D0SPA11	LPDDR3_CH1_D0SPA11	20
					DDR3L_CH1_D0S12 / LPDDR3_CH1_D0SPA12	AT5	LPDDR3_CH1_D0SPA12	LPDDR3_CH1_D0SPA12	20
					DDR3L_CH1_D0S13 / LPDDR3_CH1_D0SPA13	AT6	LPDDR3_CH1_D0SPA13	LPDDR3_CH1_D0SPA13	20
					DDR3L_CH1_D0S14 / LPDDR3_CH1_D0SPA14	BC2	LPDDR3_CH1_D0SPA14	LPDDR3_CH1_D0SPA14	20
					DDR3L_CH1_D0S15 / LPDDR3_CH1_D0SPA15	BB1	LPDDR3_CH1_D0SPA15	LPDDR3_CH1_D0SPA15	20

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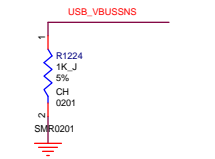
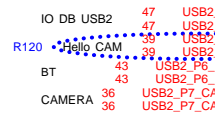
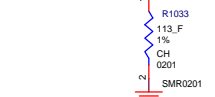
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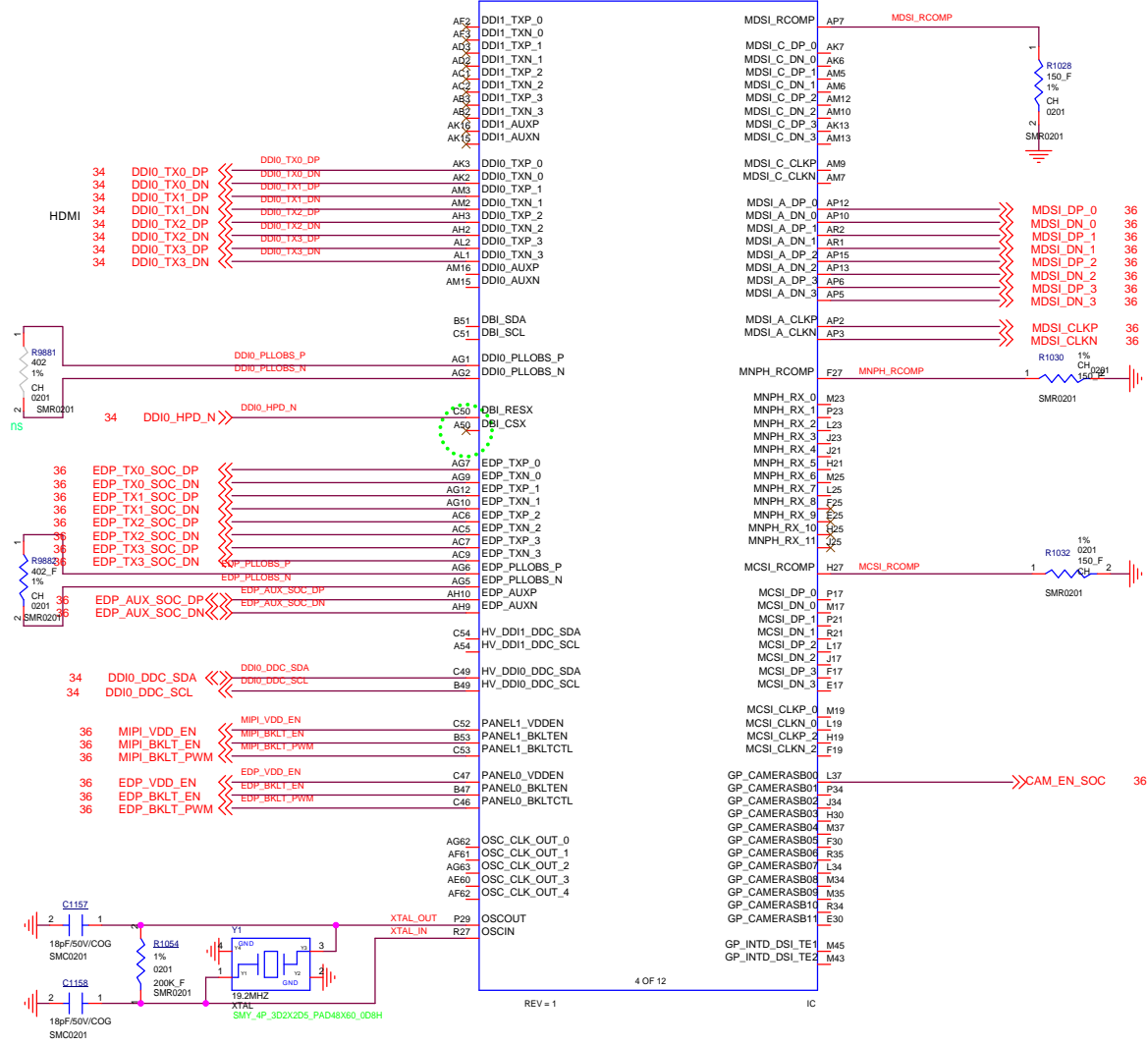
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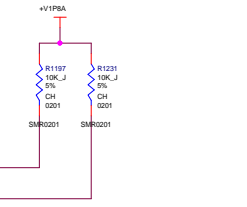
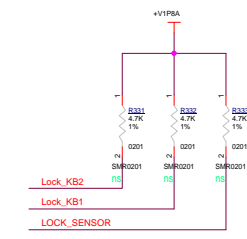
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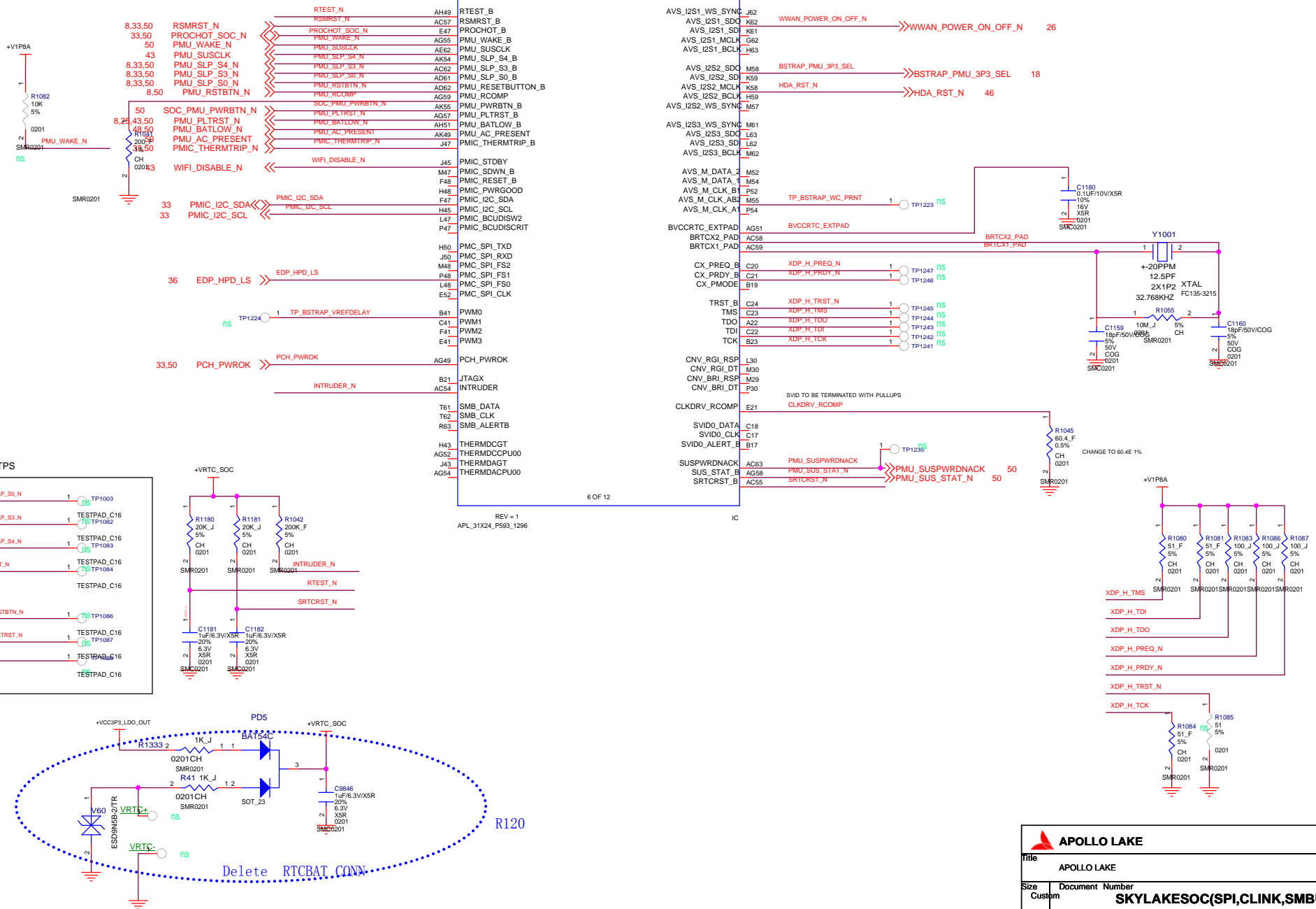


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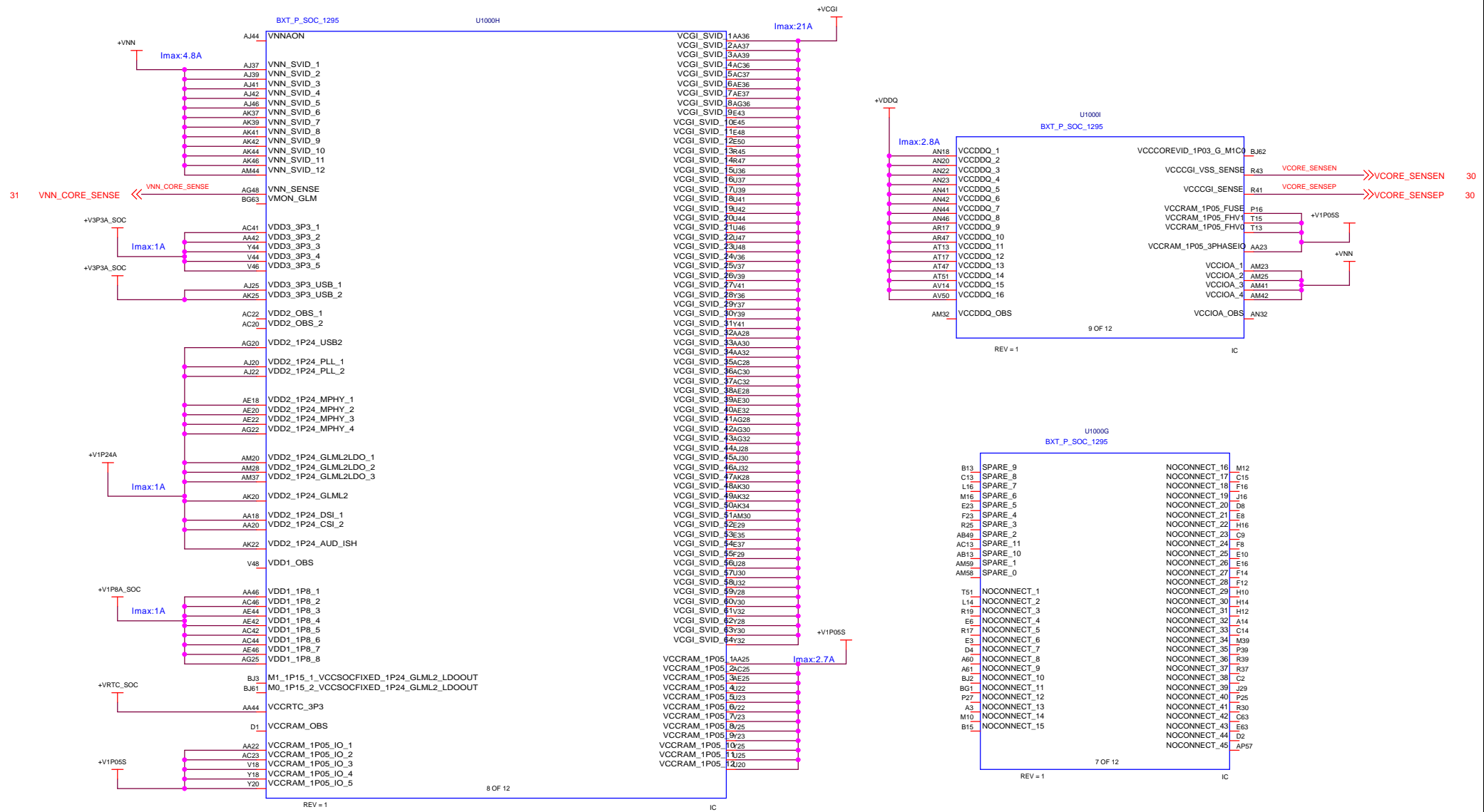
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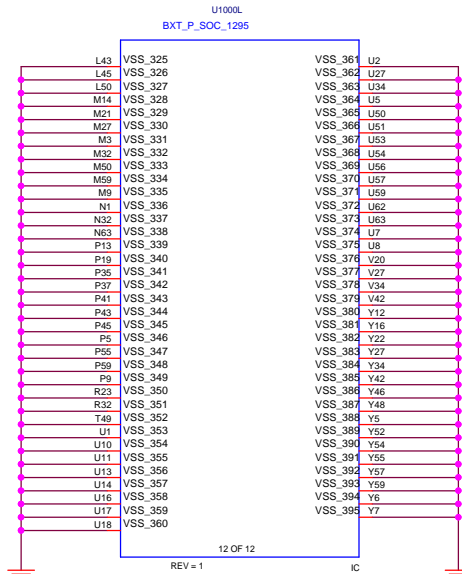
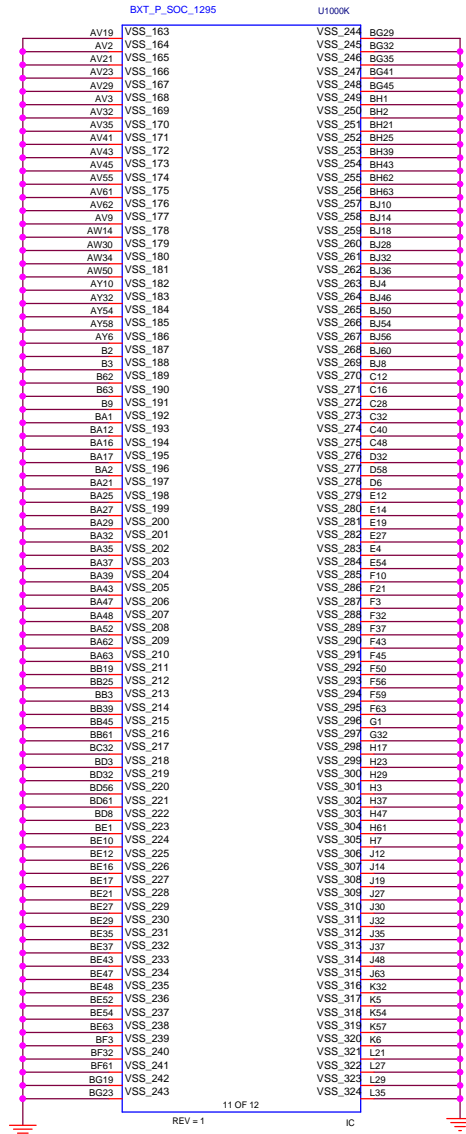
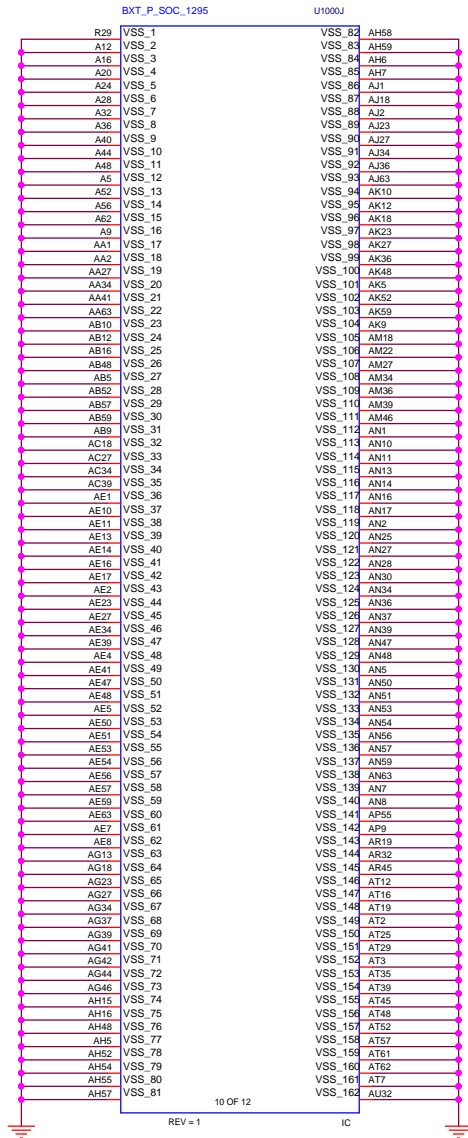


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Add RC follow EMC Request

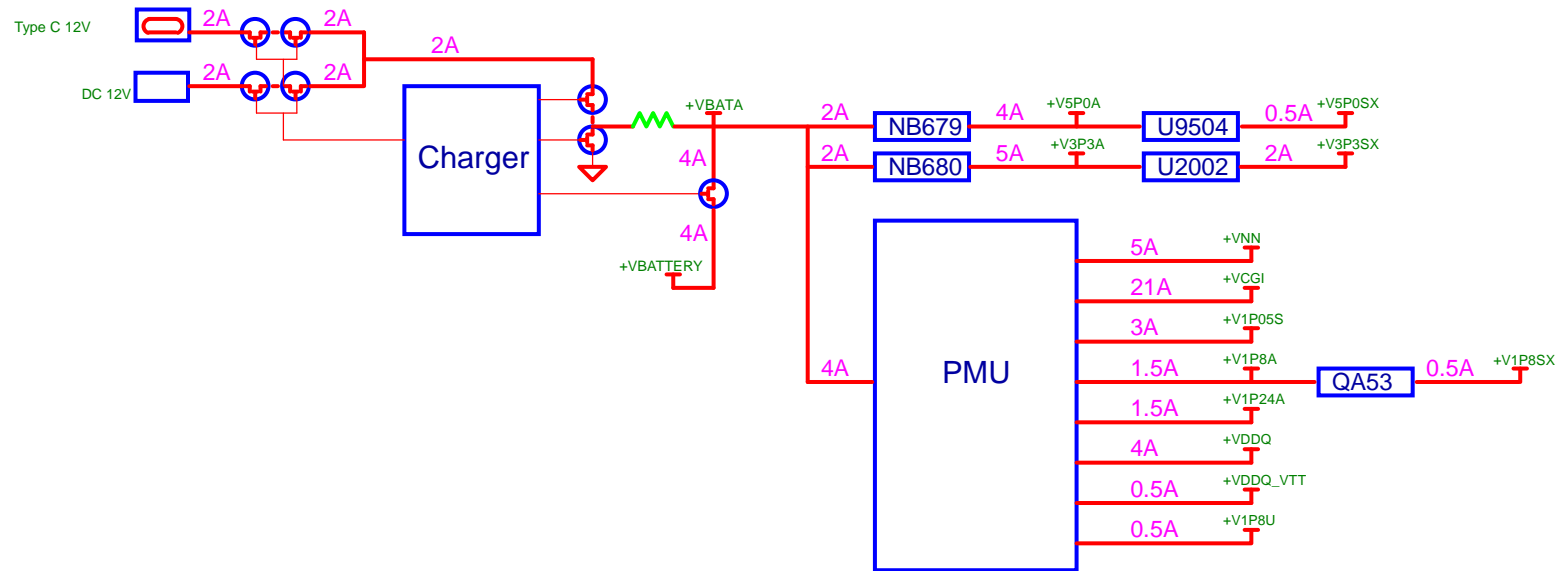


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Power Deliver




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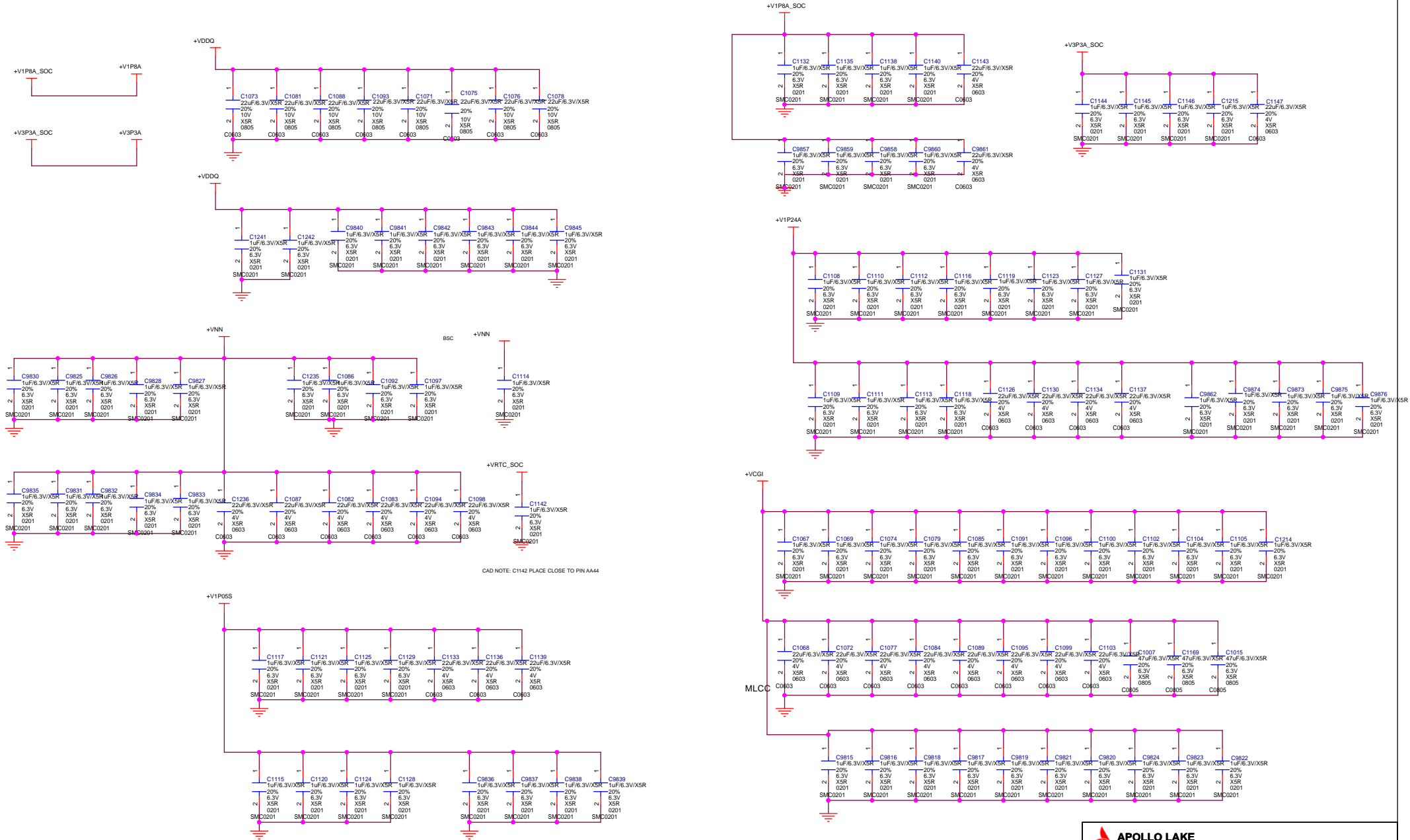
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Custom	SKYLAKE SOC (CPU MISC,JTAG)		R100
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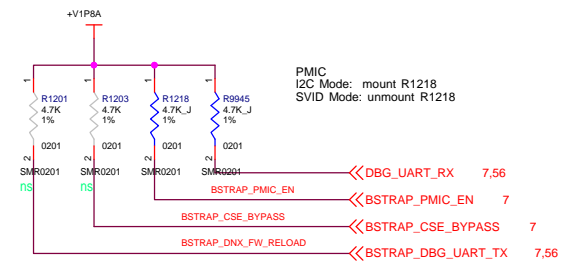
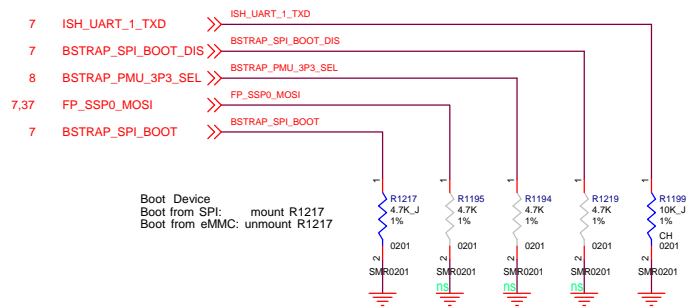
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Title APOLLO LAKE			
Size	Document Number		Rev
Custom	SKYLAKE SOC (RSVD TEST)		R100
Date:	Tuesday, December 06, 2016	Sheet	15 of 57

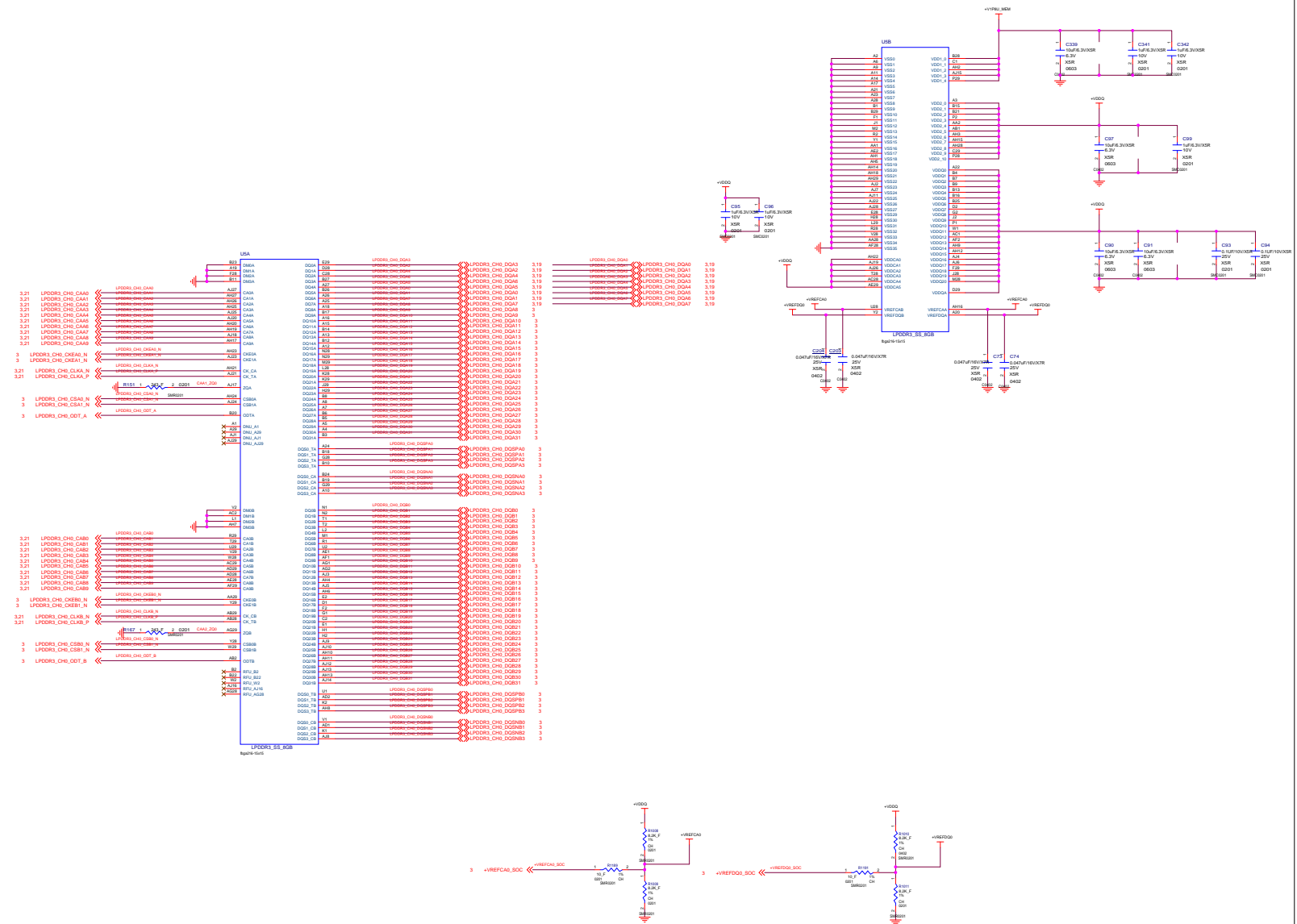
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Size	Document	Number	Rev
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Date:	Tuesday, December 06, 2016		Sheet 16 of 57

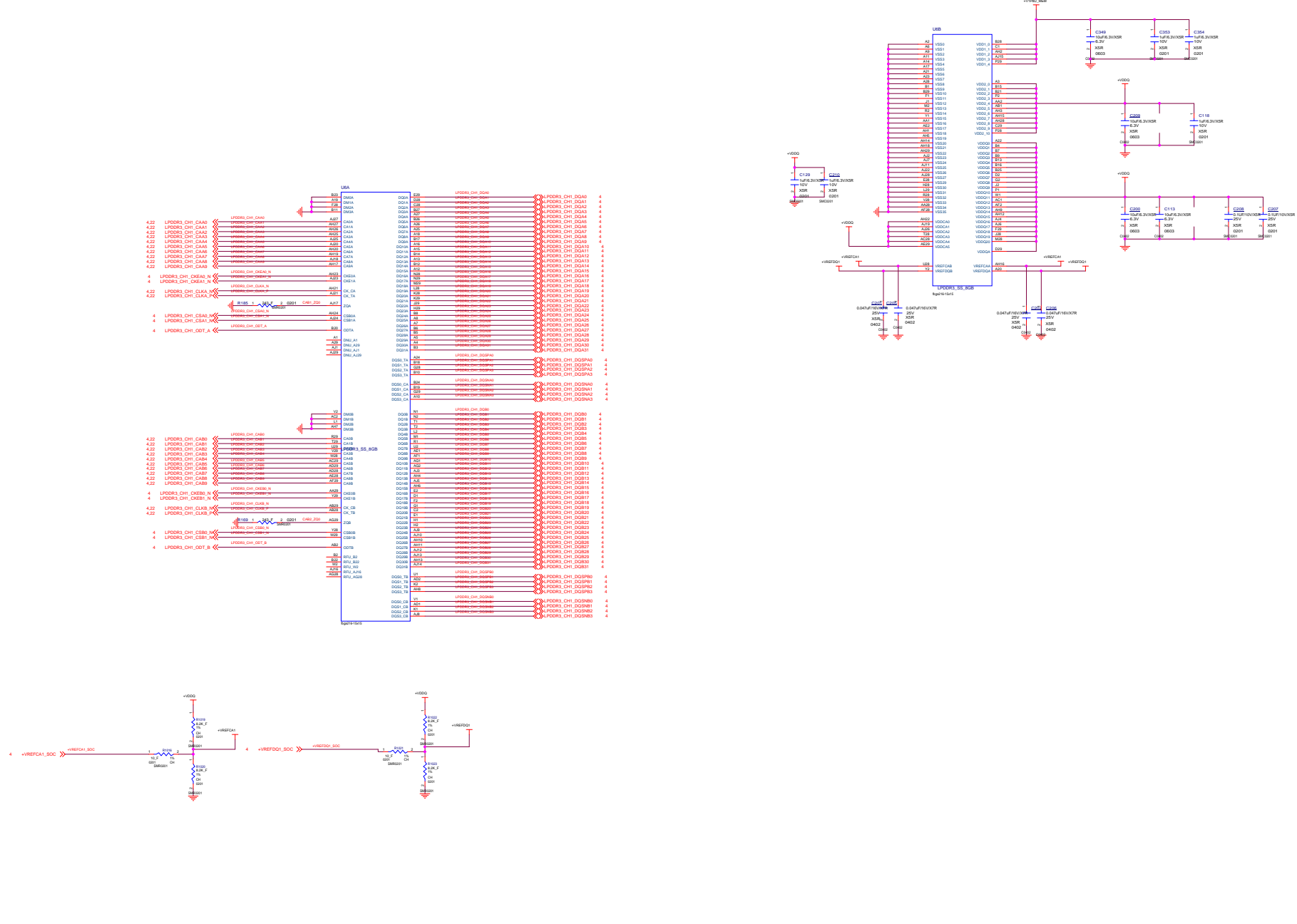


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Size	Document Number		Rev
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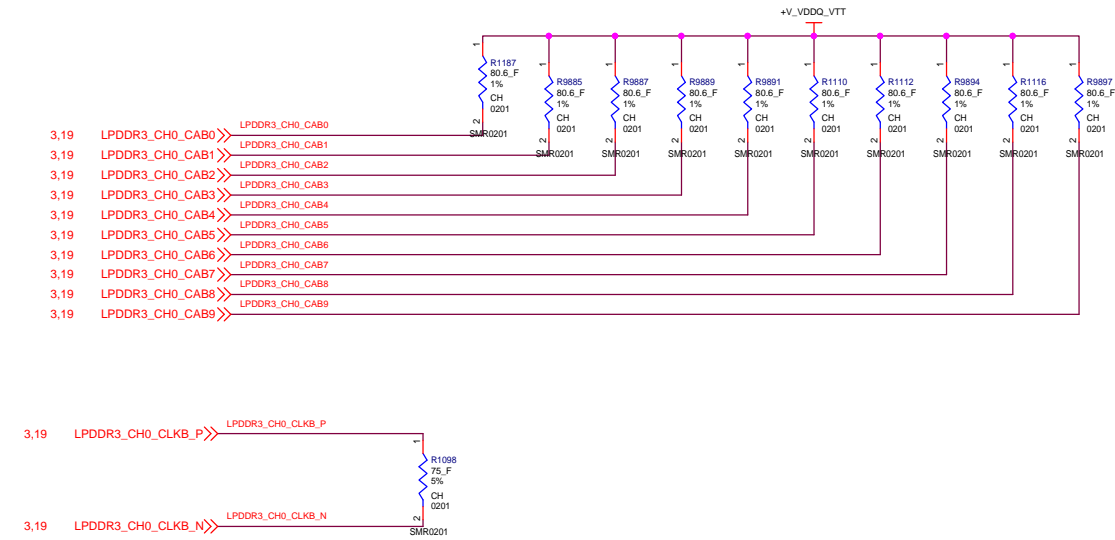
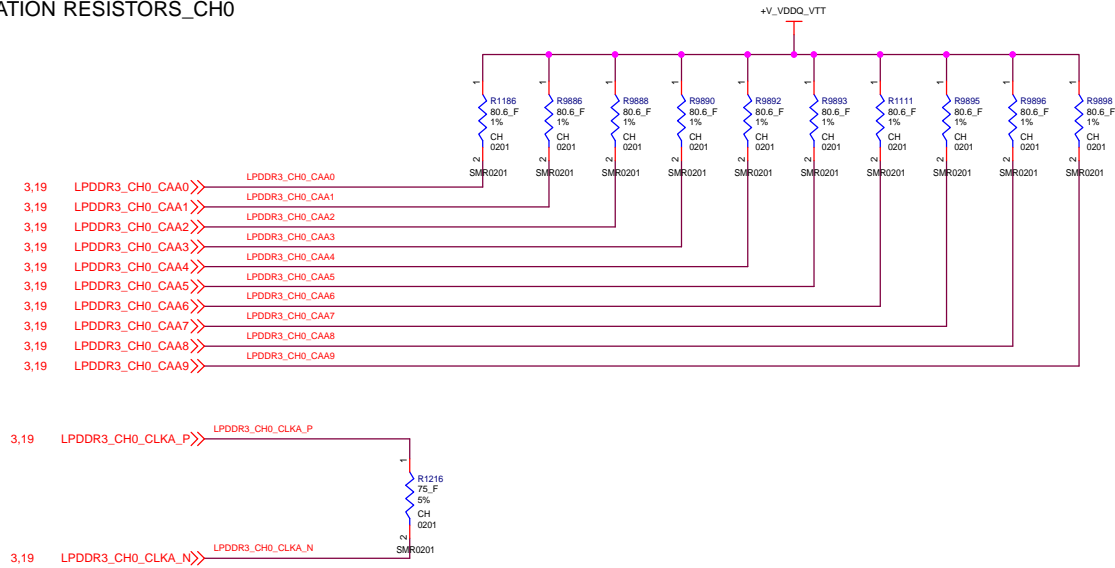




Pin	Internal Node	Internal Node	Internal Node
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804	DQA1	LPDDR3_CH_DQA1	LPDDR3_CH_DQA1
805	DQA2	LPDDR3_CH_DQA2	LPDDR3_CH_DQA2
806	DQA3	LPDDR3_CH_DQA3	LPDDR3_CH_DQA3
807	DQA4	LPDDR3_CH_DQA4	LPDDR3_CH_DQA4
808	DQA5	LPDDR3_CH_DQA5	LPDDR3_CH_DQA5
809	DQA6	LPDDR3_CH_DQA6	LPDDR3_CH_DQA6
810	DQA7	LPDDR3_CH_DQA7	LPDDR3_CH_DQA7
811	DQA8	LPDDR3_CH_DQA8	LPDDR3_CH_DQA8
812	DQA9	LPDDR3_CH_DQA9	LPDDR3_CH_DQA9
813	DQA10	LPDDR3_CH_DQA10	LPDDR3_CH_DQA10
814	DQA11	LPDDR3_CH_DQA11	LPDDR3_CH_DQA11
815	DQA12	LPDDR3_CH_DQA12	LPDDR3_CH_DQA12
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817	DQA14	LPDDR3_CH_DQA14	LPDDR3_CH_DQA14
818	DQA15	LPDDR3_CH_DQA15	LPDDR3_CH_DQA15
819	DQA16	LPDDR3_CH_DQA16	LPDDR3_CH_DQA16
820	DQA17	LPDDR3_CH_DQA17	LPDDR3_CH_DQA17
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823	DQA20	LPDDR3_CH_DQA20	LPDDR3_CH_DQA20
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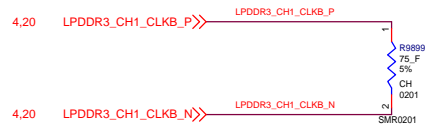
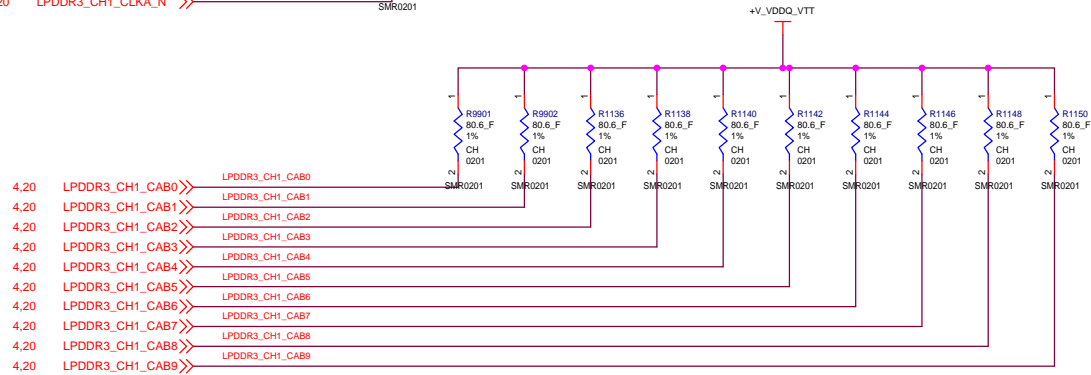
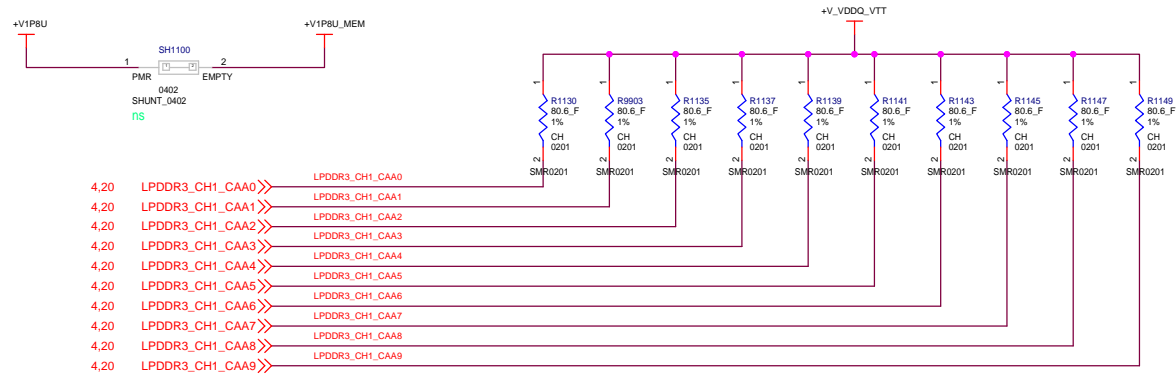


LPDDR3L-RS TERMINATION RESISTORS_CH0

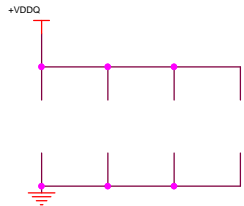
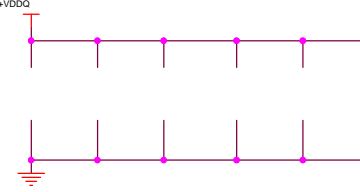
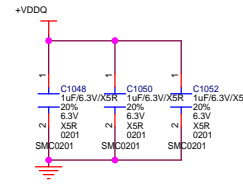
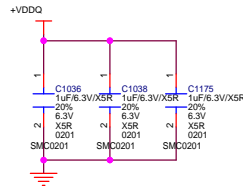
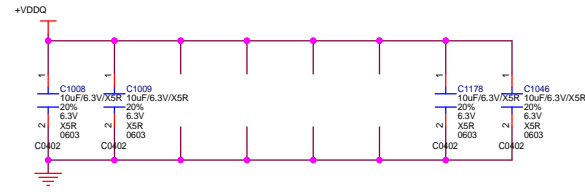
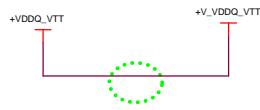


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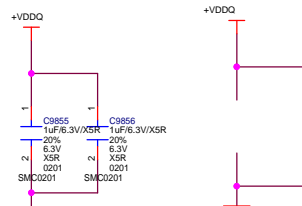
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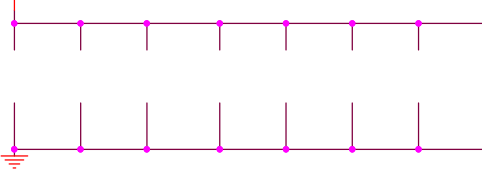
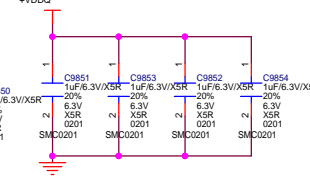
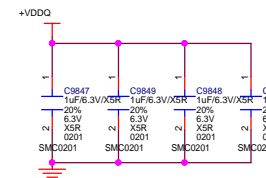
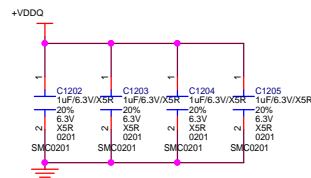
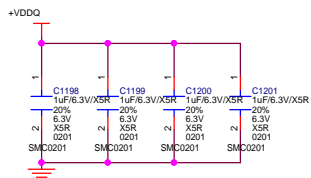
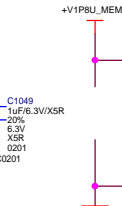
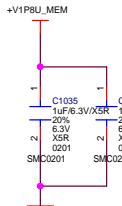
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Size Custom	Document Number LPDDR3 CH-A DEVICE-1		Rev R100
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FOUR 0402 IN MID CHANNEL

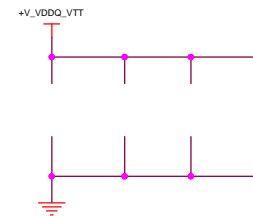
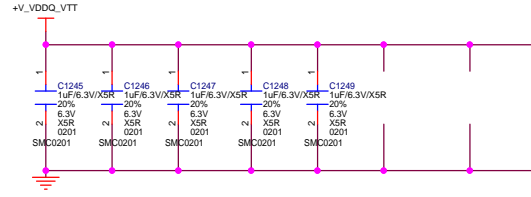
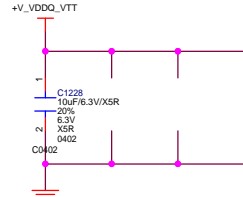
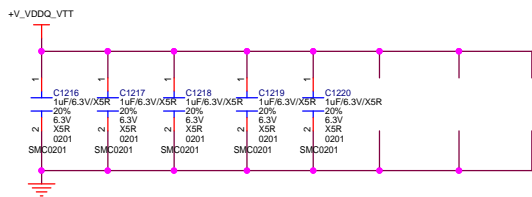


TWO 0402 ON EACH END CHANNEL

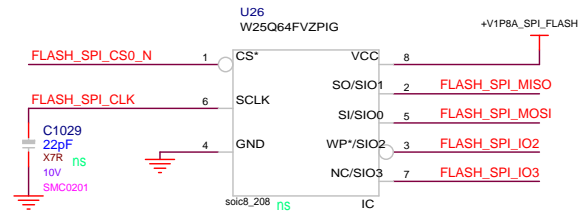
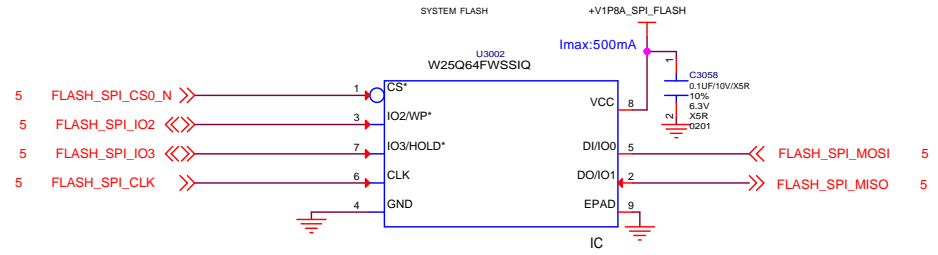
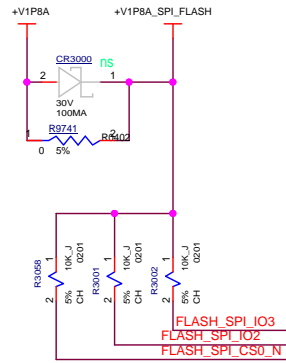


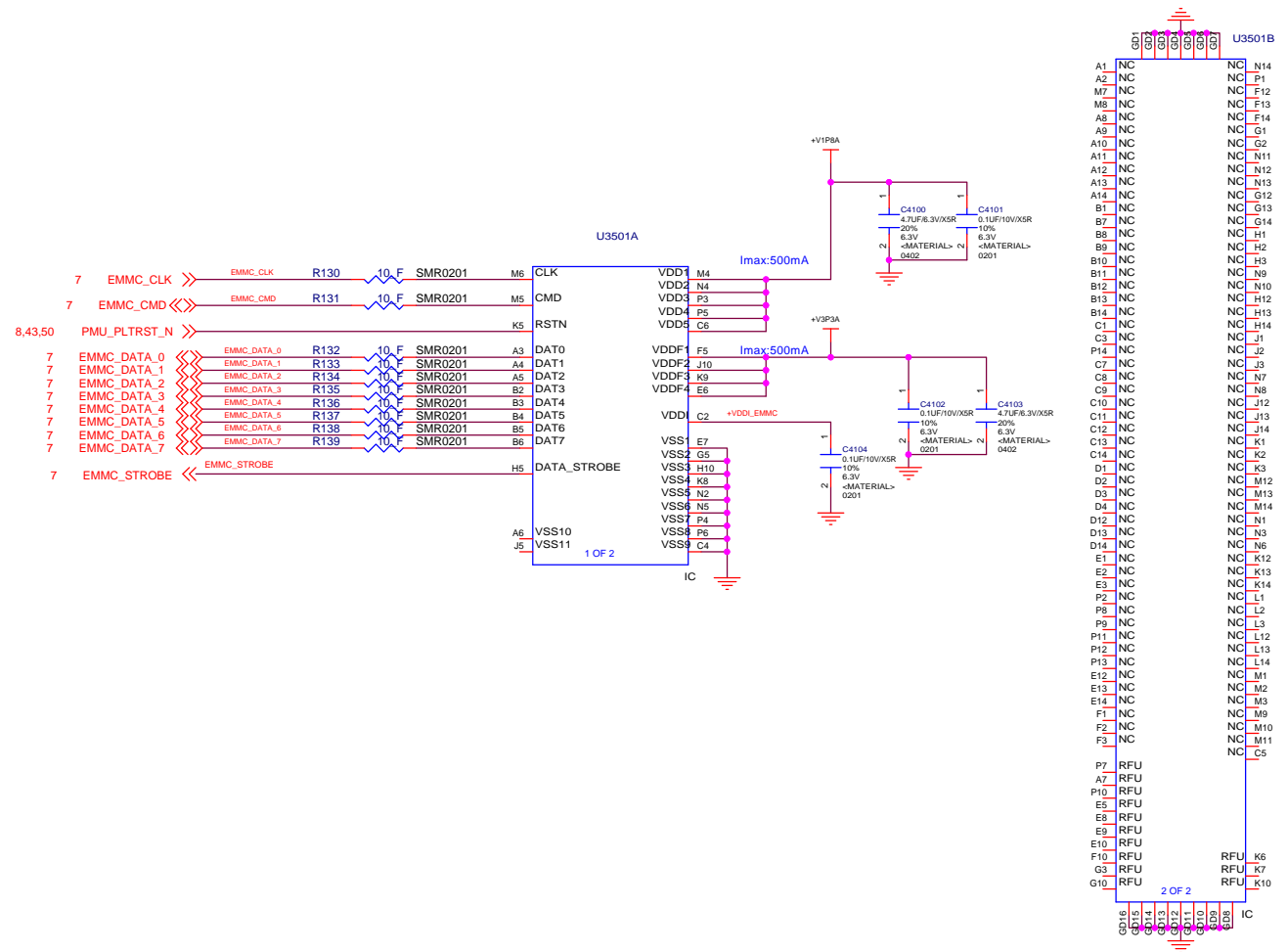
NOTE: PLACE ON TOP - 4 PER DEVICE

NOTE: PLACE ON TOP - 4 PER DEVICE

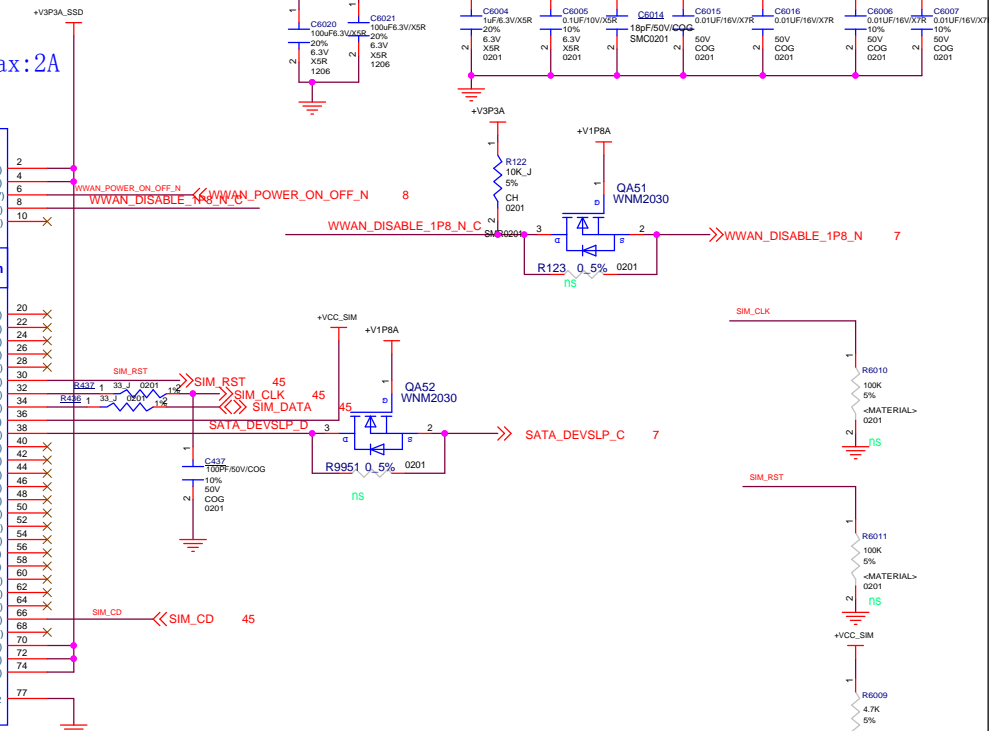
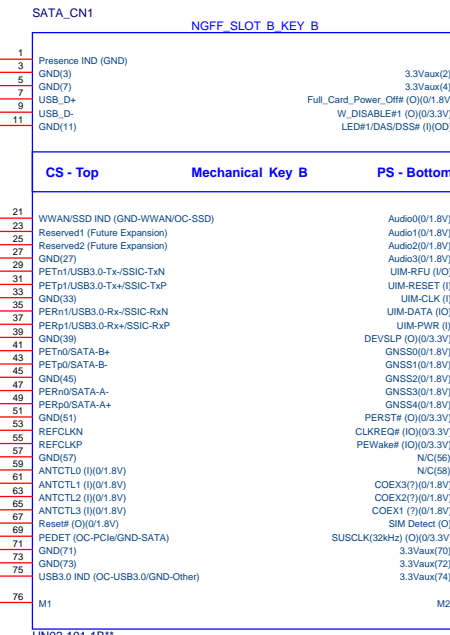
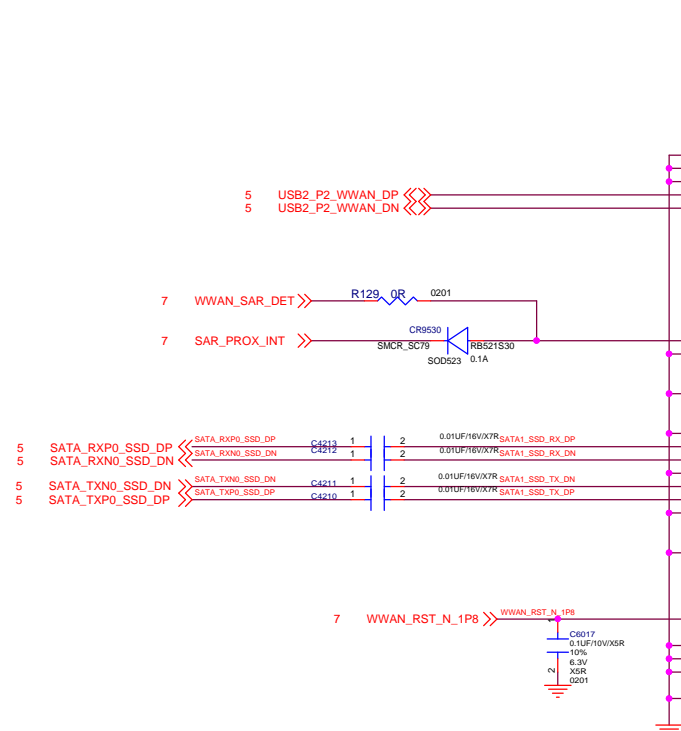
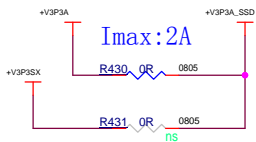


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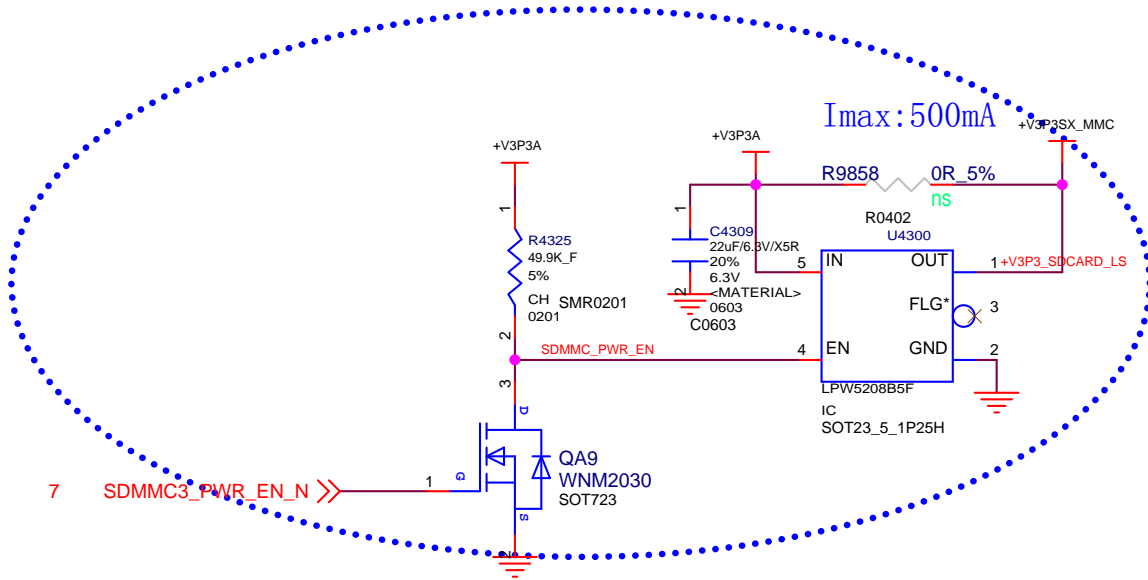
Title APOLLO LAKE			
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NGFF SOCKET (M.2) RVS B KEY
NGFF_CON75-S-HN02-101-1


Title: APOLLO LAKE		
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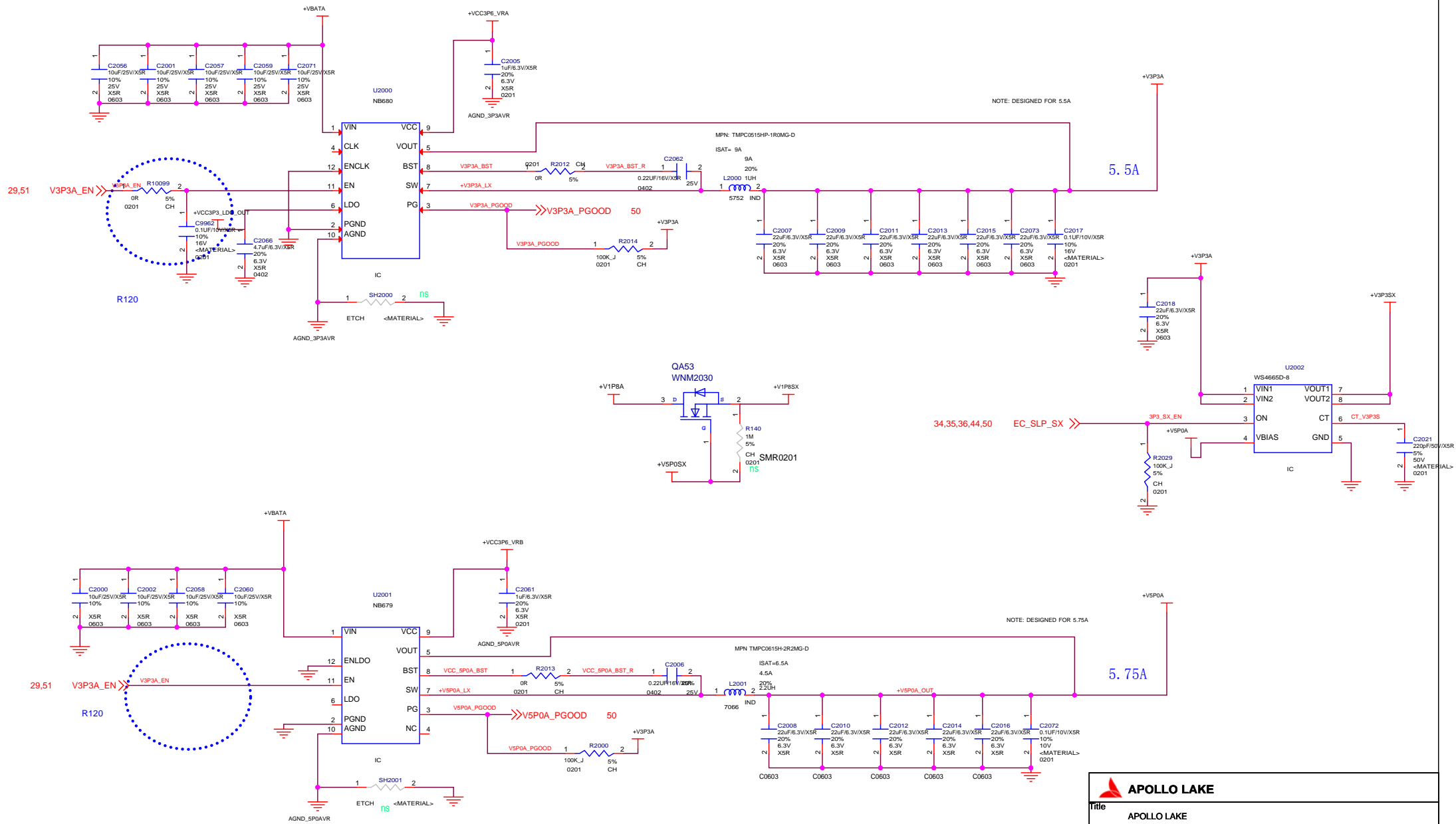
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Title		
APOLLO LAKE		
Size	Document Number	Rev
B	MICRO-SD CARD	R100
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Imax: 500mA

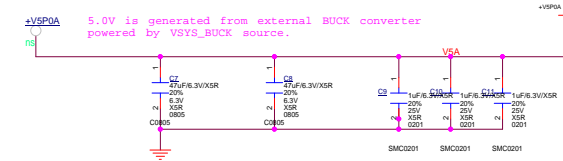
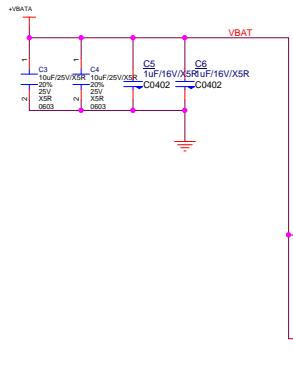
R120
Use USB2.0 transfer to TF , R9858 Install, U4300 NS

 APOLLO LAKE		
Title		
APOLLO LAKE		
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A	SDCARD POWER	R100
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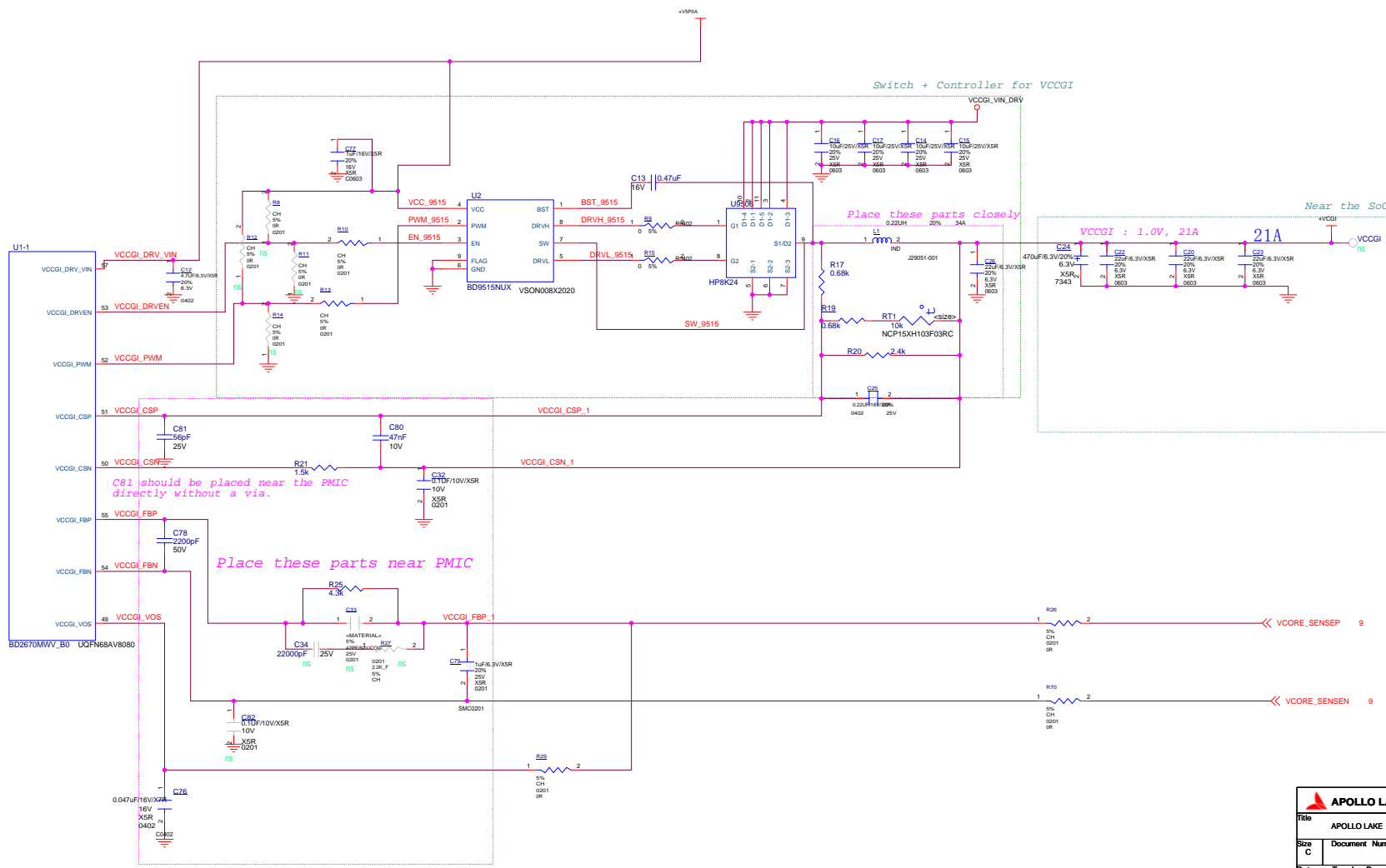


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POWER DELIVERY 5V AND 3.3V			
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2S/3S battery input [5.4V to 21V]



Connect to VCCGI High-Side Switch [4A]
 Connect to VSYS pin of BD2670MMV [typ.:8uA, max: 20 - 30uA]



C81 should be placed near the PMIC directly without a via.

Place these parts near PMIC

Switch + Controller for VCCGI

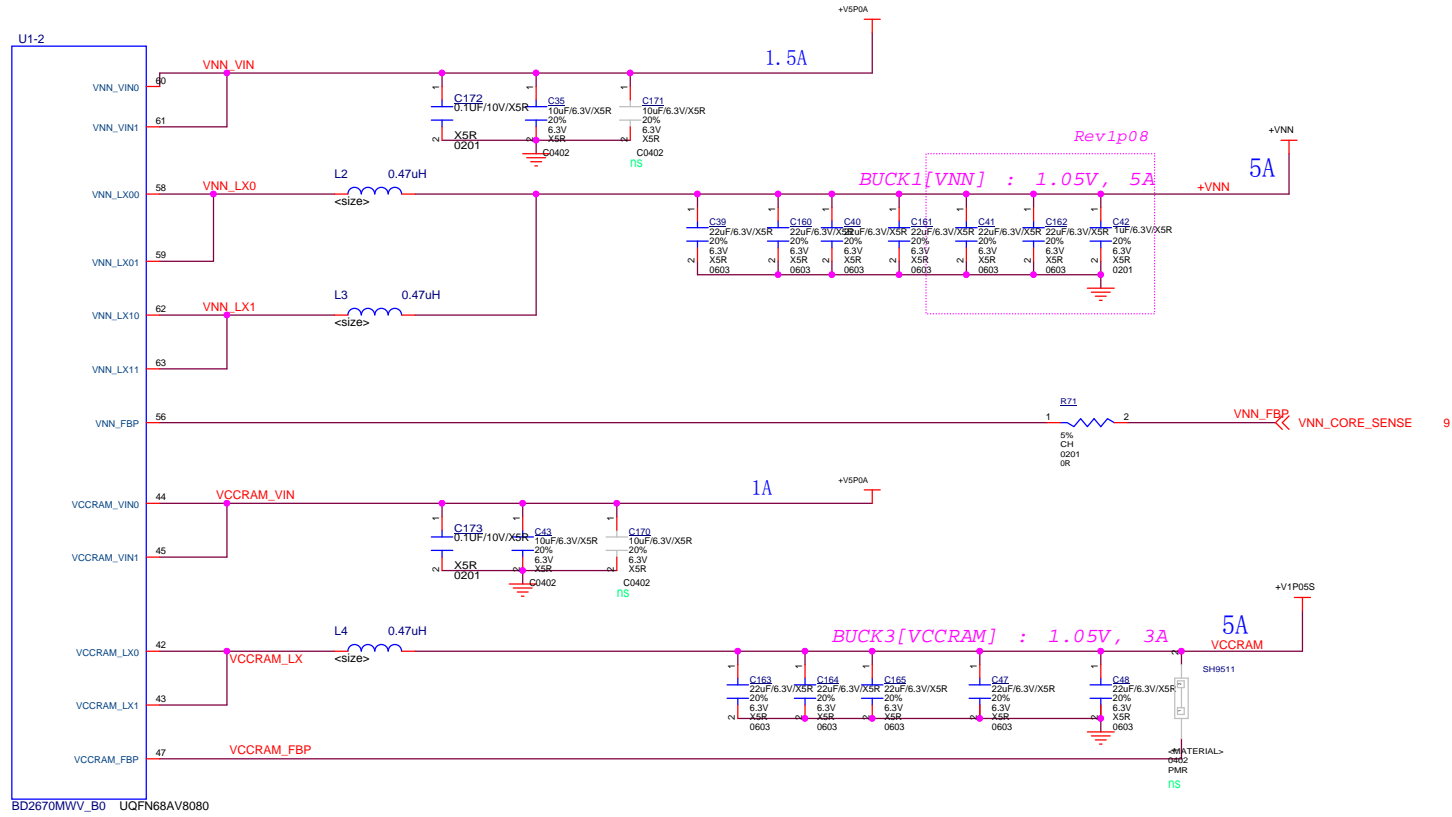
Place these parts closely

Near the SoC

VCCGI : 1.0V, 21A

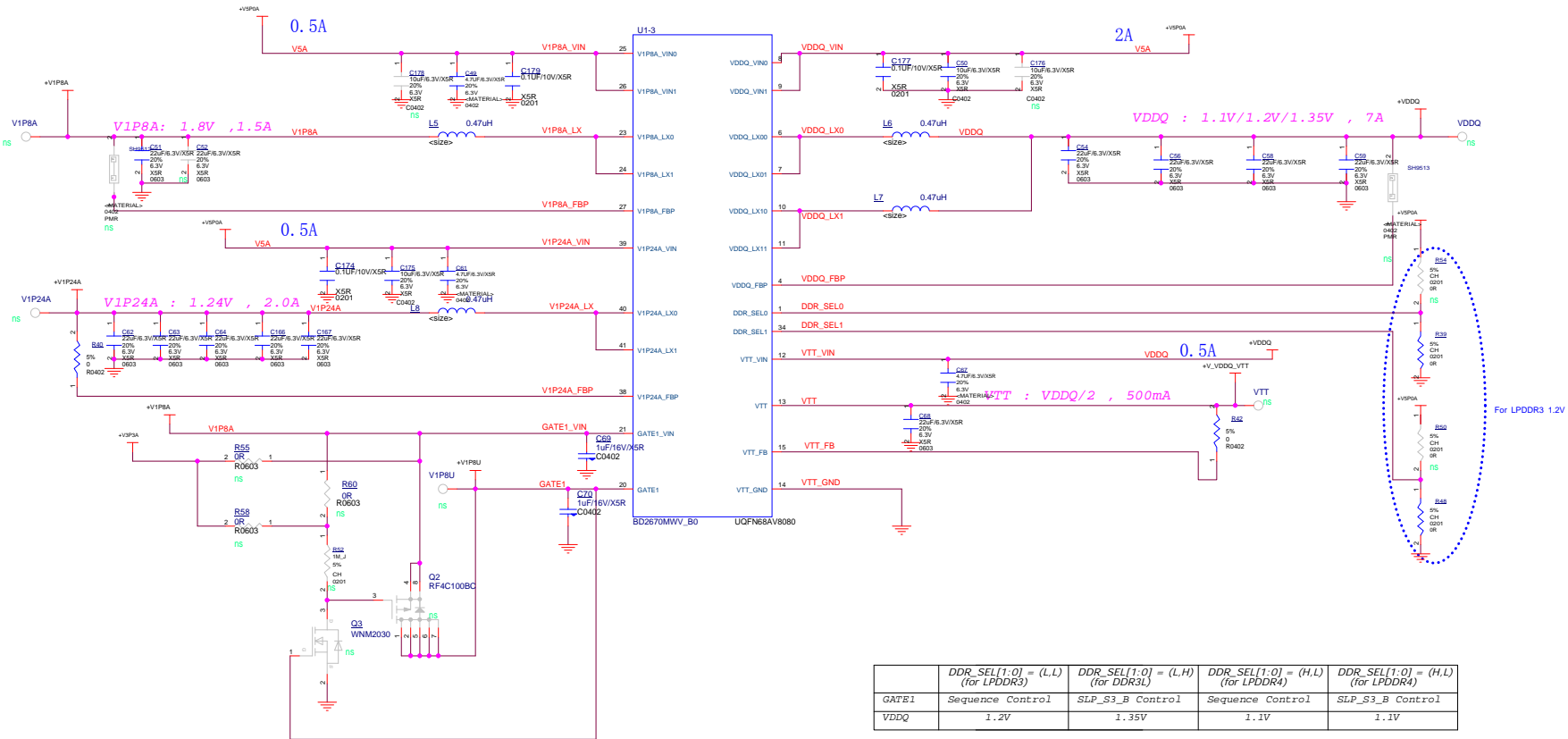
21A

VNN[BUCK1], VCCRAM[BUCK3]

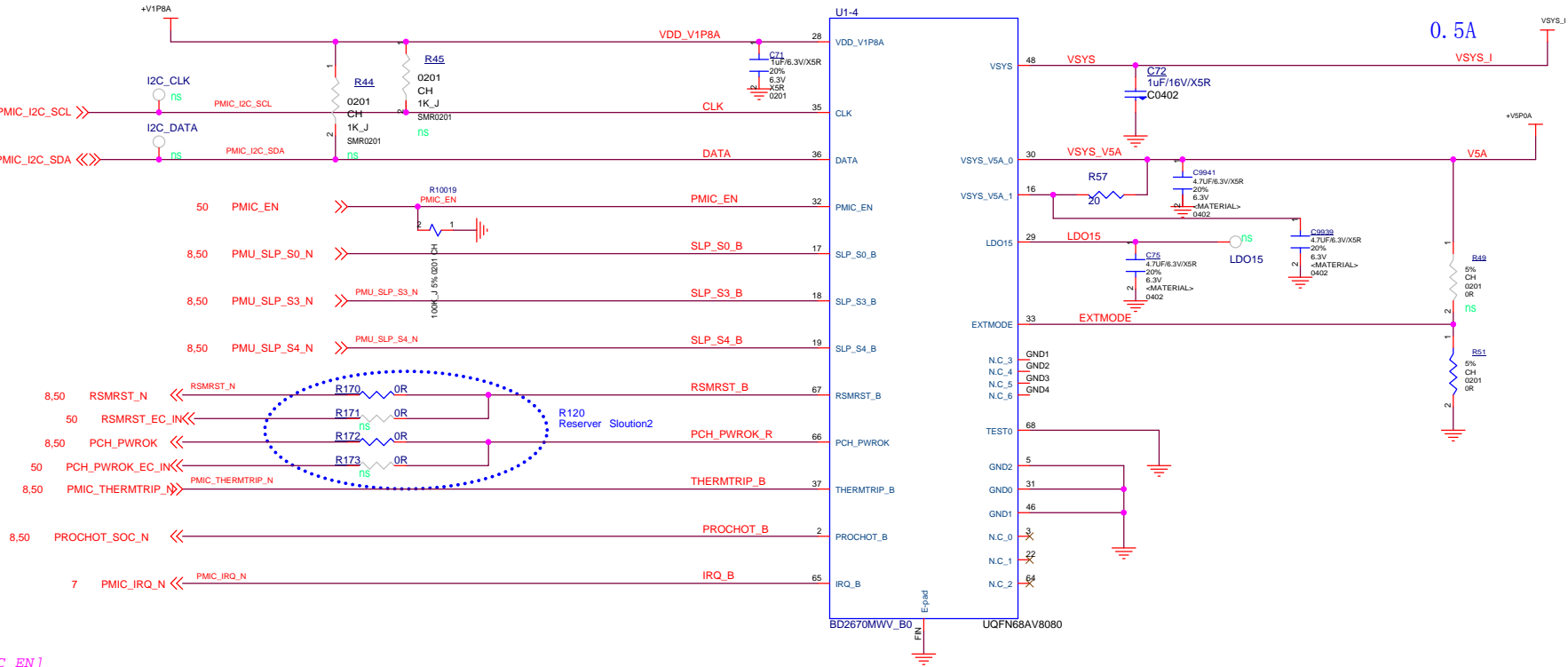


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V1P8A[BUCK4], V1P24A[BUCK5], VDDQ[BUCK6]



I2C , Other signals

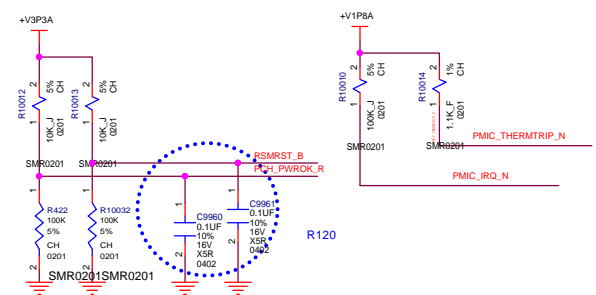


0.5A

[PMIC_EN]
Connected to EC.

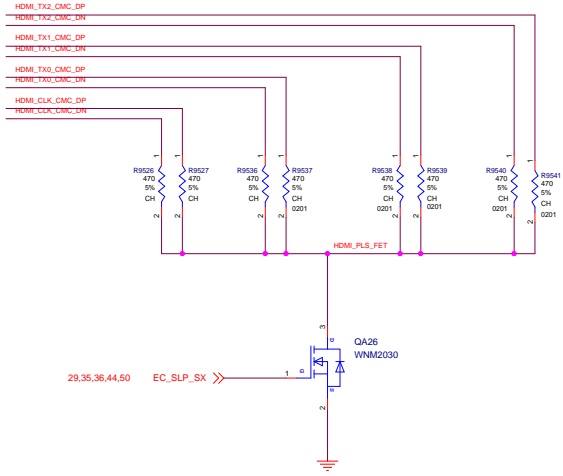
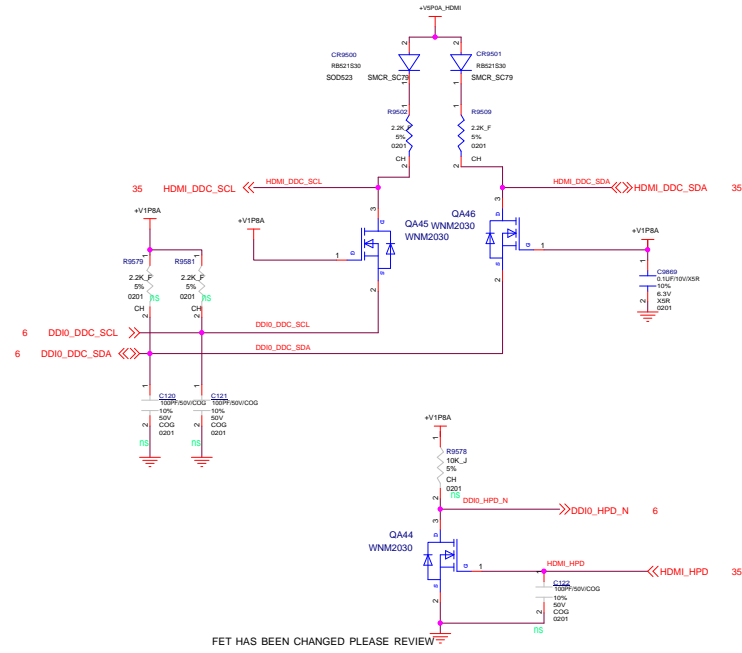
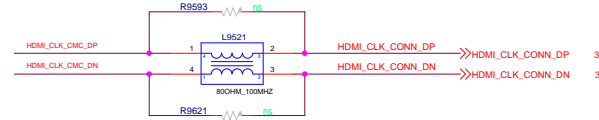
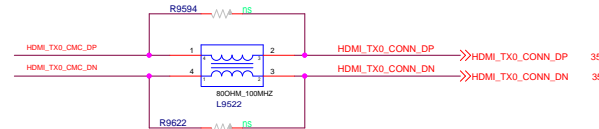
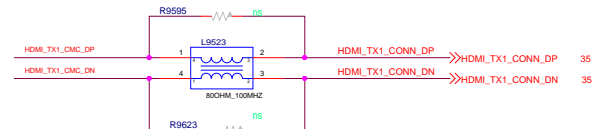
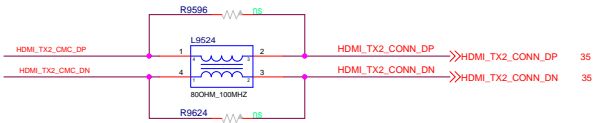
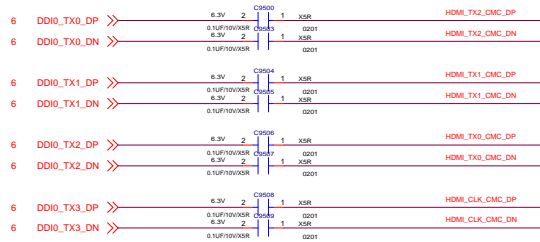
[PCH_PWROK, RSMRST_B, PROCHOT_B, IRQ_B]
These pins are open drain outputs and need pull-up resistors according to the condition of the connected devices.

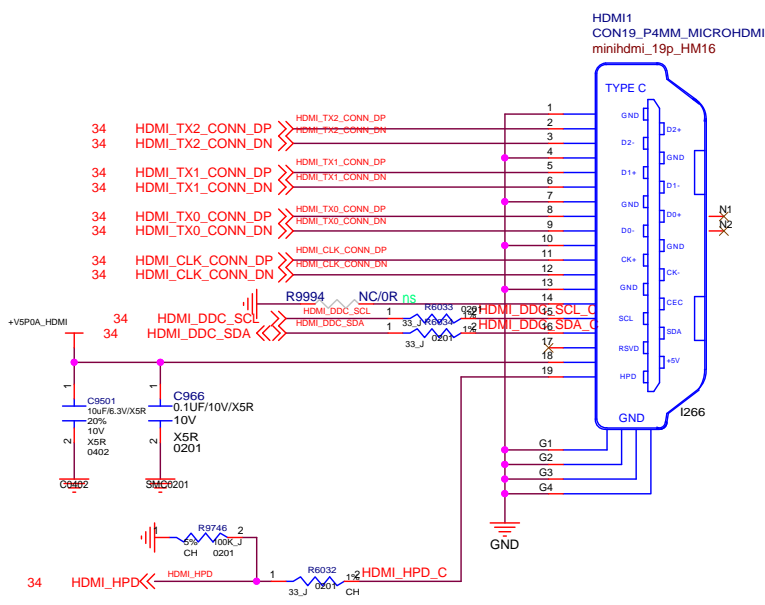
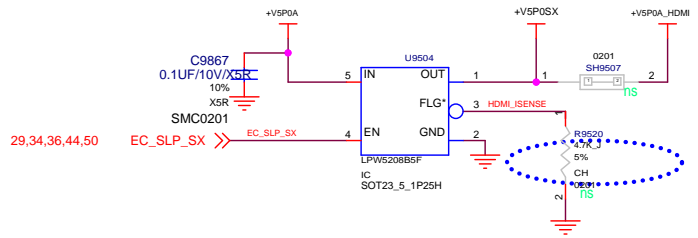
[SLP_S0_B, SLP_S3_B, SLP_S4_B, THERMTRIP_B]
Connected to SoC.



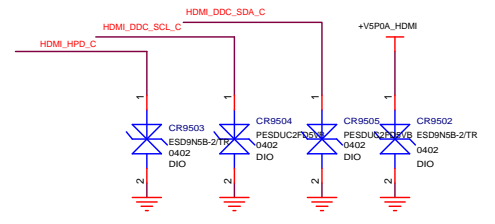
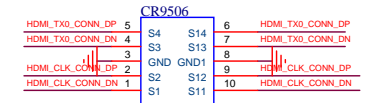
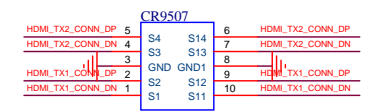
Title APOLLO LAKE			
Size	Document Number	Rev	
Custom	POWER DELIVERY1.8V AND 1.0V	R100	
Date:	Tuesday, December 06, 2016	Sheet	33 of 57

HDMI LEVEL SHIFTERS & CONNECTOR





Change to MINI HDMI

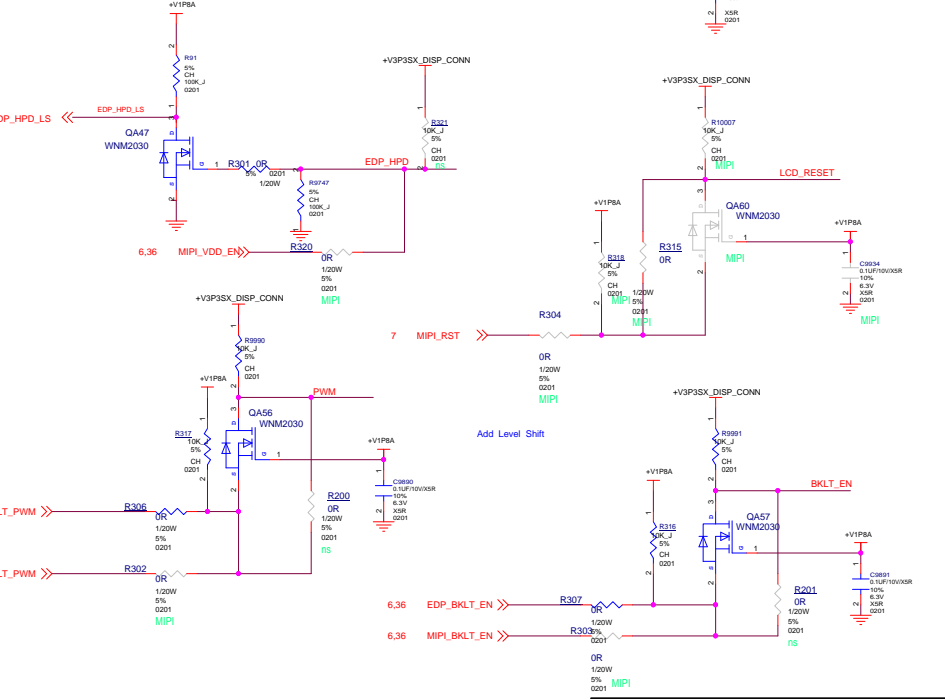
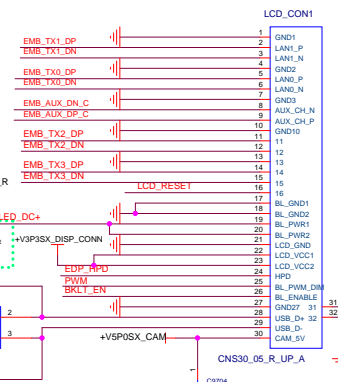
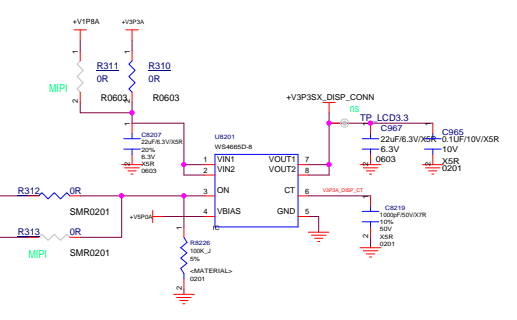
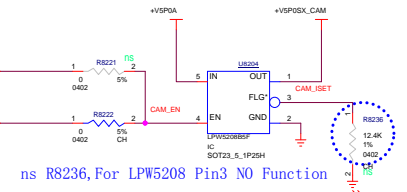
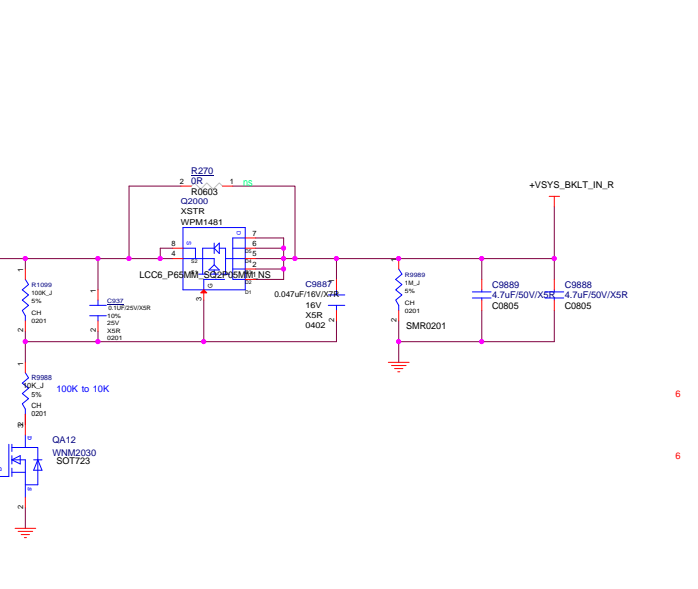
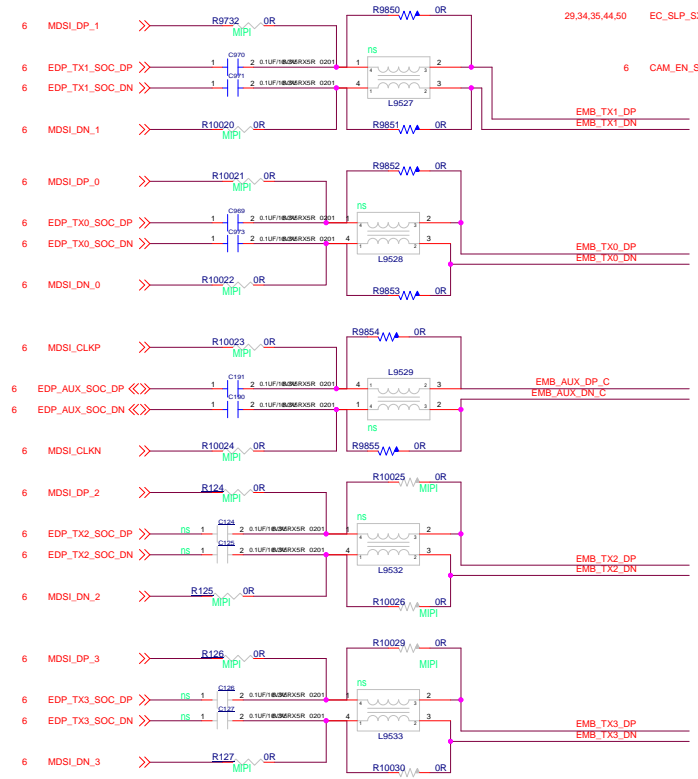


Title	APOLLO LAKE	
Size B	Document Number HDMI CONNECTOR	Rev R100
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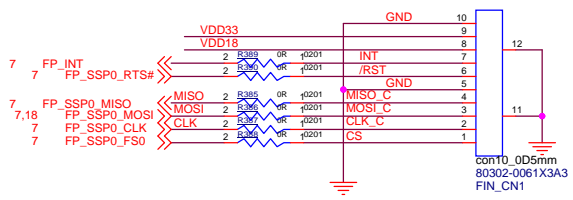
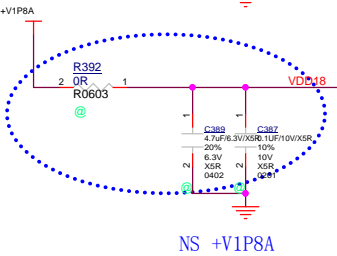
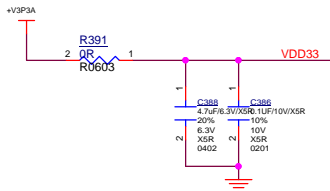
T65	EDP_HPD
T66	EMB_AUX_DP_C
T67	EMB_AUX_DN_C
T72	EMB_TX1_DP
T73	EMB_TX1_DN
T74	EMB_TX0_DP
T75	EMB_TX0_DN


D42	EMB_TX1_DP	S14	S4	5	EMB_TX1_DP
	EMB_TX1_DN	S15	S4	4	EMB_TX1_DN
	GND1	GND	3		
	EMB_TX0_DP	S12	S2	2	EMB_TX0_DP
	EMB_TX0_DN	S11	S1	1	EMB_TX0_DN

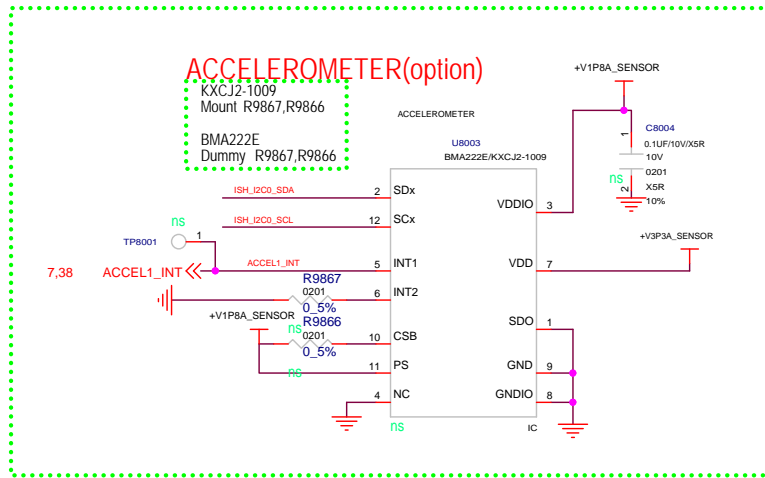
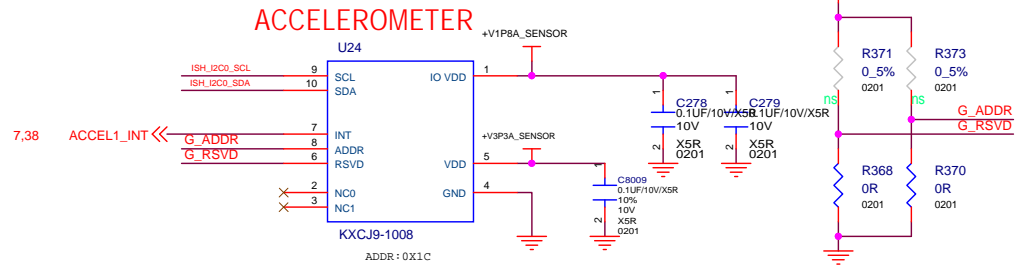
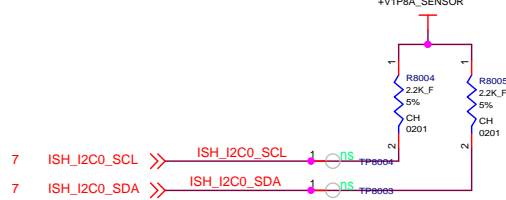
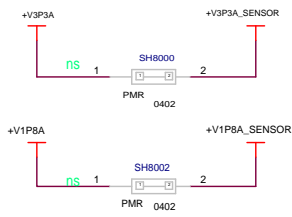
D43	EMB_TX2_DP	S14	S4	5	EMB_TX2_DP
	EMB_TX2_DN	S15	S4	4	EMB_TX2_DN
	GND1	GND	3		
	EMB_TX3_DP	S12	S2	2	EMB_TX3_DP
	EMB_TX3_DN	S11	S1	1	EMB_TX3_DN



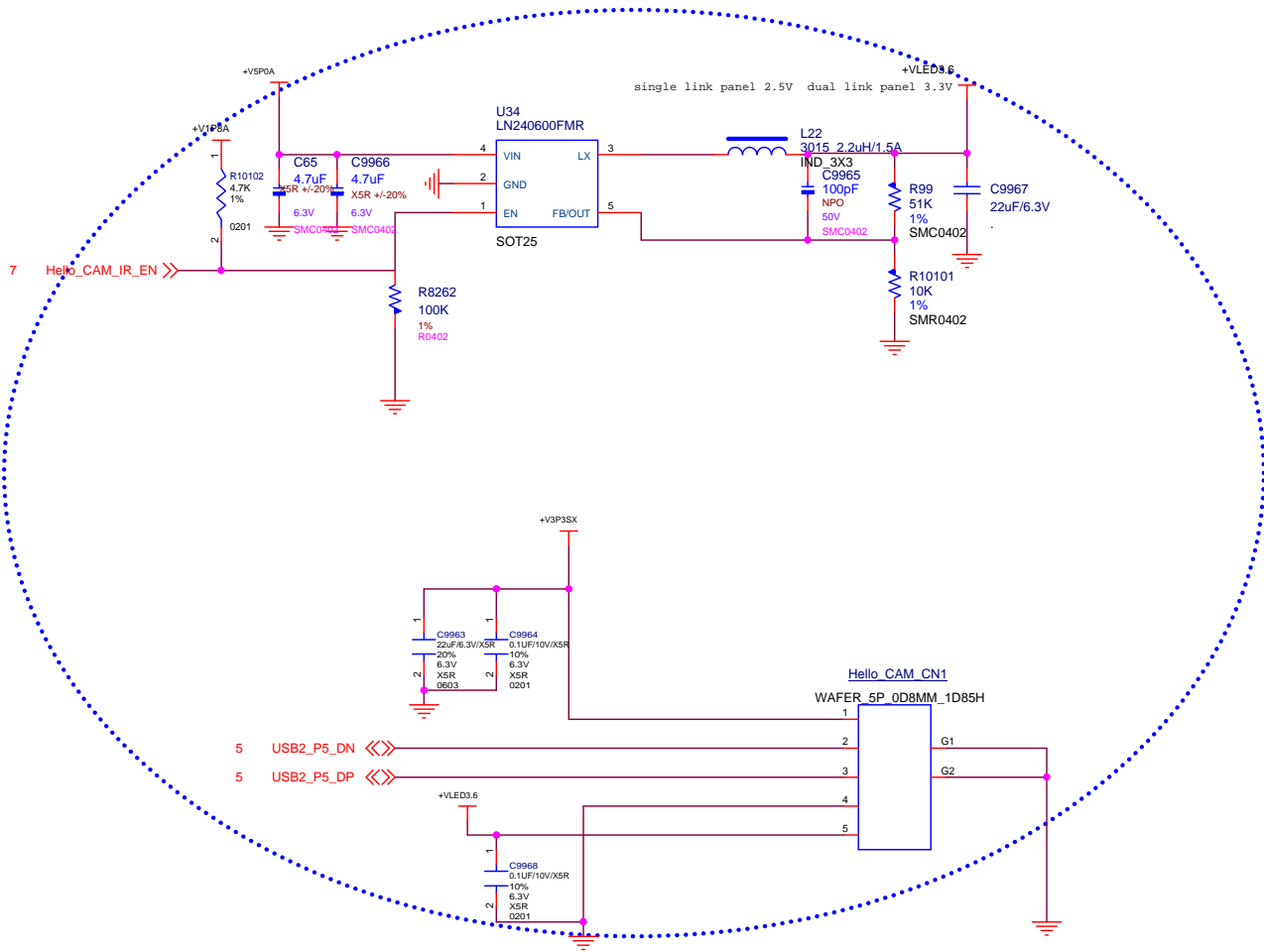
APOLLO LAKE	
APOLLO LAKE	
Size C	Document Number
DISPLAY/TP(EDP CN)	
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Title			
APOLLO LAKE			
Size	Document	Number	Rev
Custom	TOUCH PANEL AND DOCK		R100
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Title			
APOLLO LAKE			
Size	Document	Number	Rev
B	SENSORS		R100
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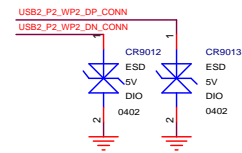
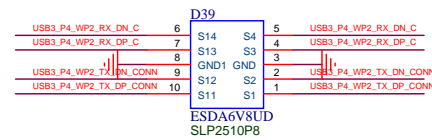
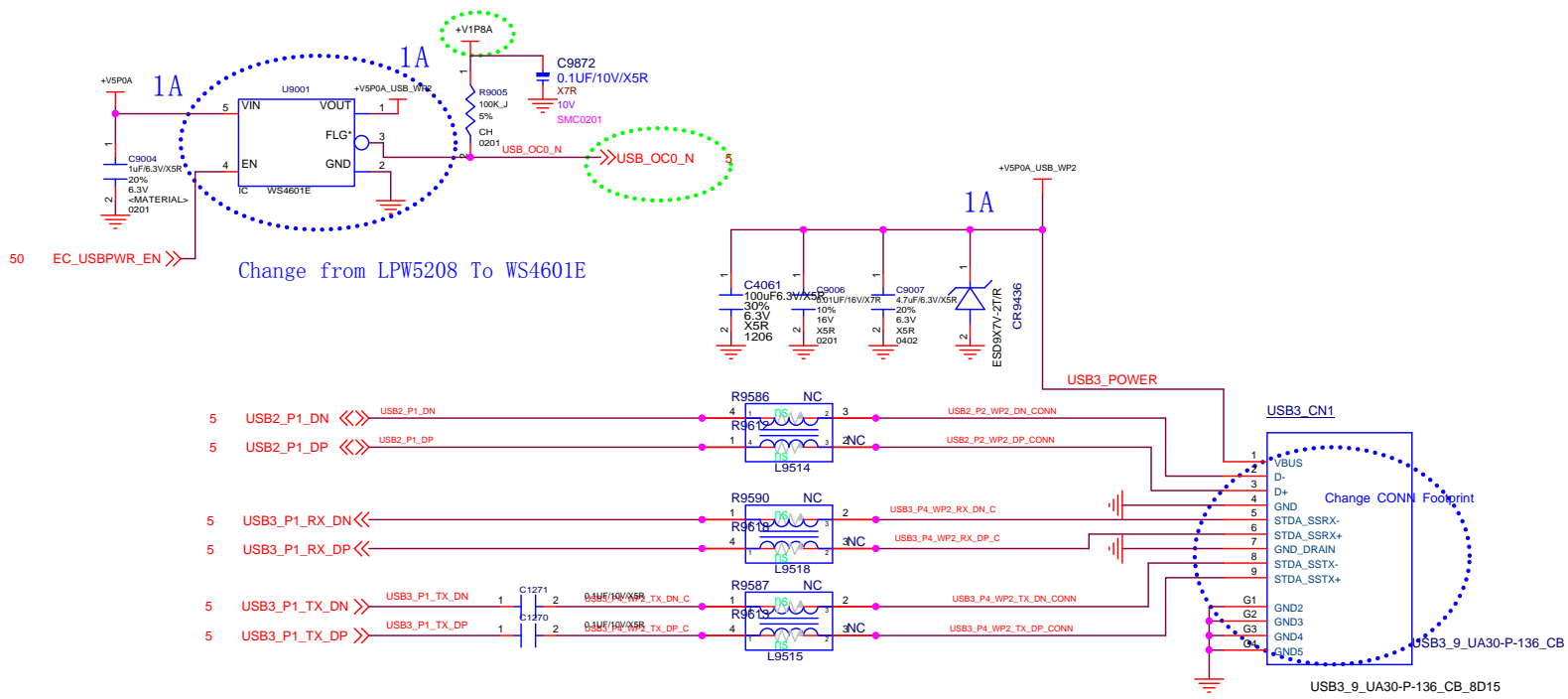


R120
Add Hello CAM

		
Title APOLLO LAKE		
Size B	Document Number FRONT AND REAR CAMERA CONN	Rev R100
Date:	Friday, December 09, 2016	Sheet 39 of 57

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Title			
APOLLO LAKE			
Size	Document	Number	Rev
B	CAMERA DISCRETE CNTRL LOGIC		R100
Date:	Tuesday, December 06, 2016	Sheet	40 of 57

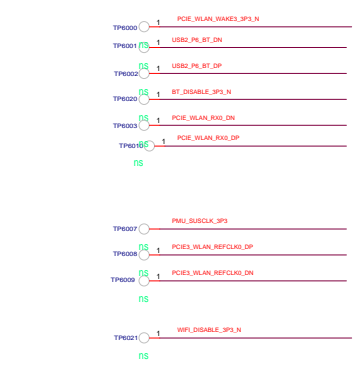
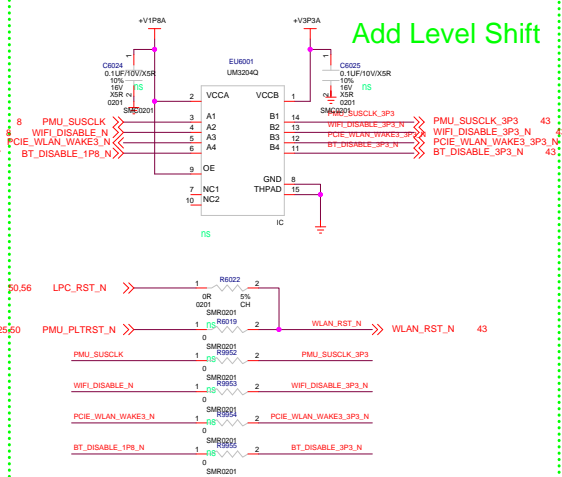
 APOLLO LAKE			
Title			
APOLLO LAKE			
Size	Document	Number	Rev
Custom	COB TP		R100
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Title		
APOLLO LAKE		
Size	Document Number	Rev
B	USB3.0 CONN	R100
Date:	Tuesday, December 06, 2016	Sheet 42 of 57

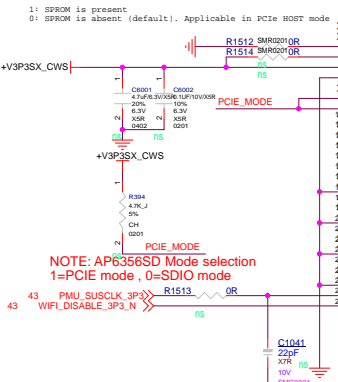
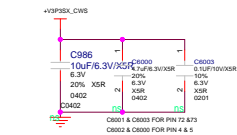


Add Level Shift

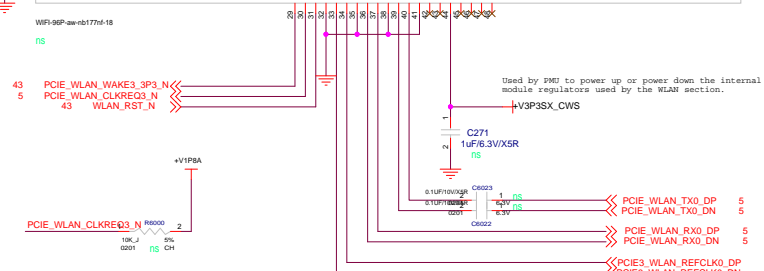
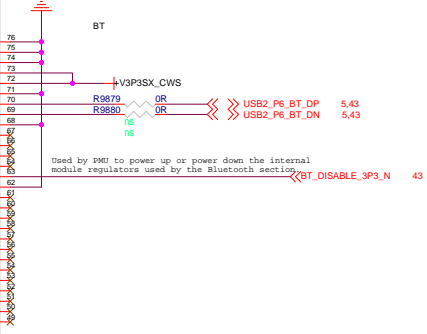
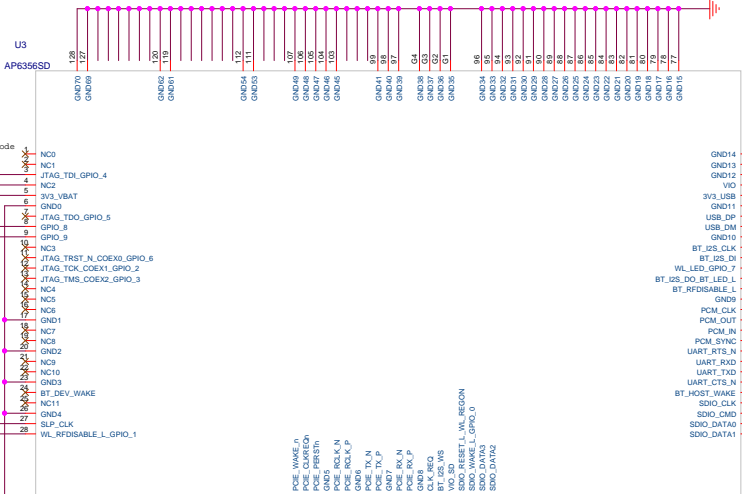
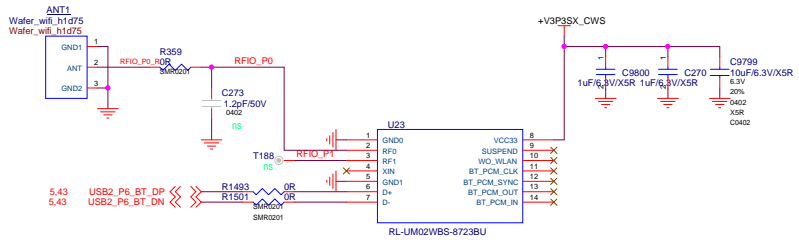


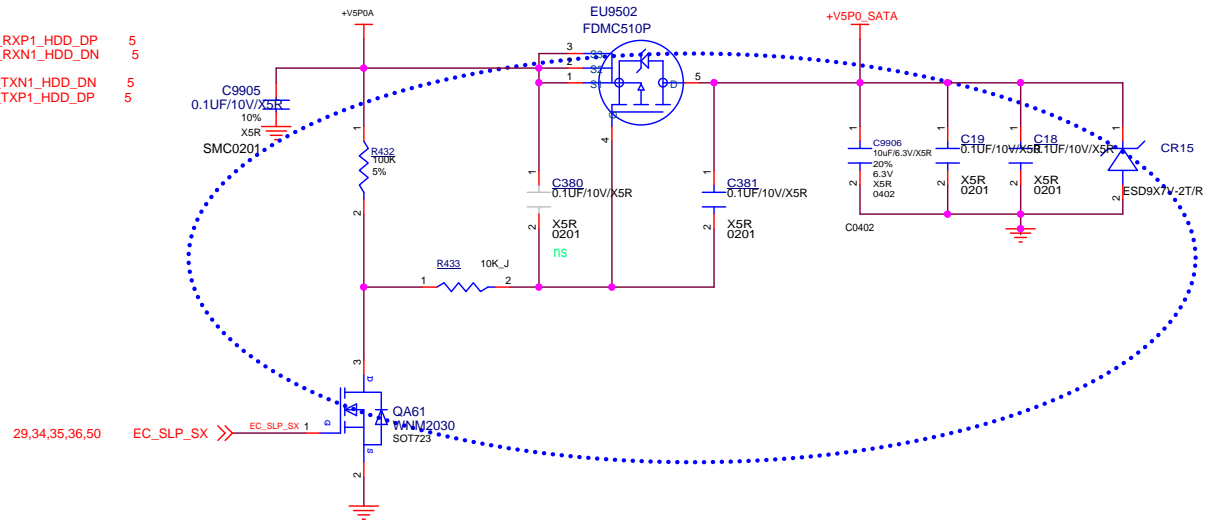
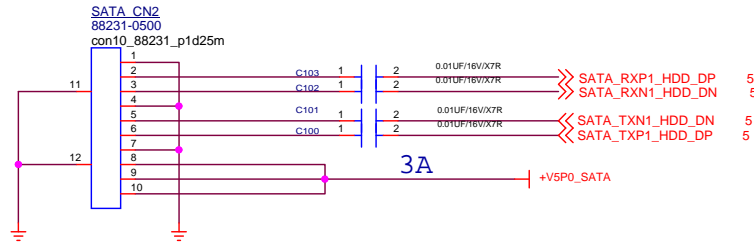
NOTE:
If WiFi interface is SDIO V2.0/3.0, the VIO must be 1.8V.
If selecting PCIe, the VIO must be tied to 3.3V

PIN	SDIO	PCIe
GPIO8	0	1
GPIO9	0	1
VIO	Tie to 1.8V	Tie to 3.3V

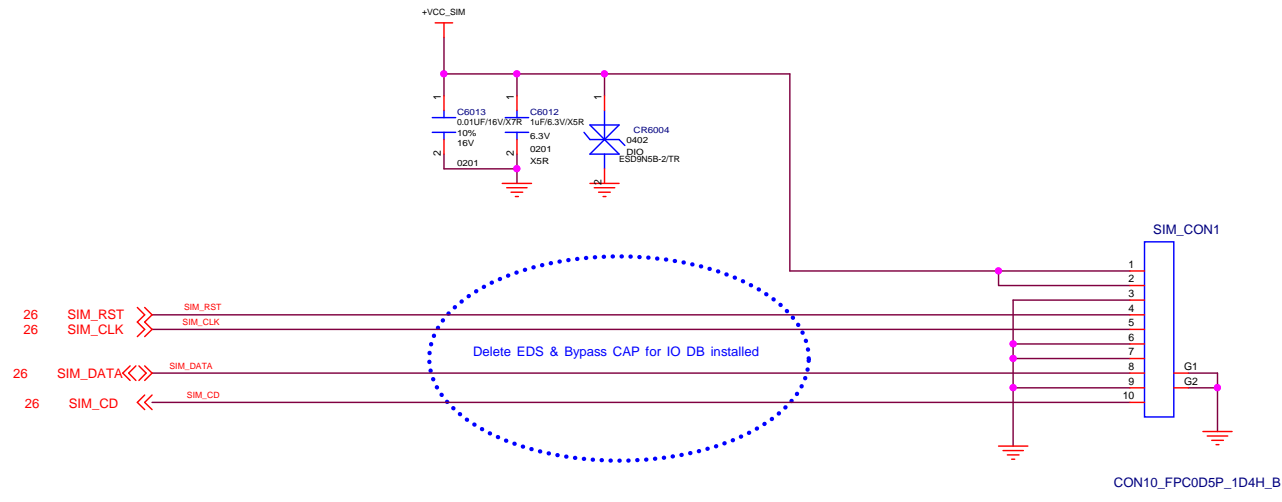



NOTE: AP6356SD Mode selection
1=PCIe mode, 0=SDIO mode

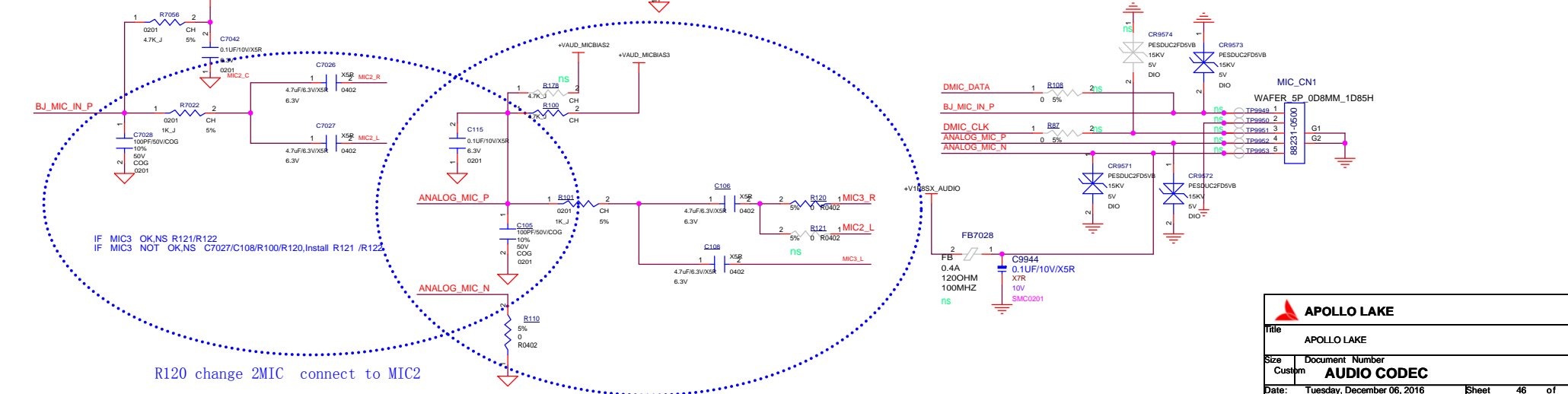
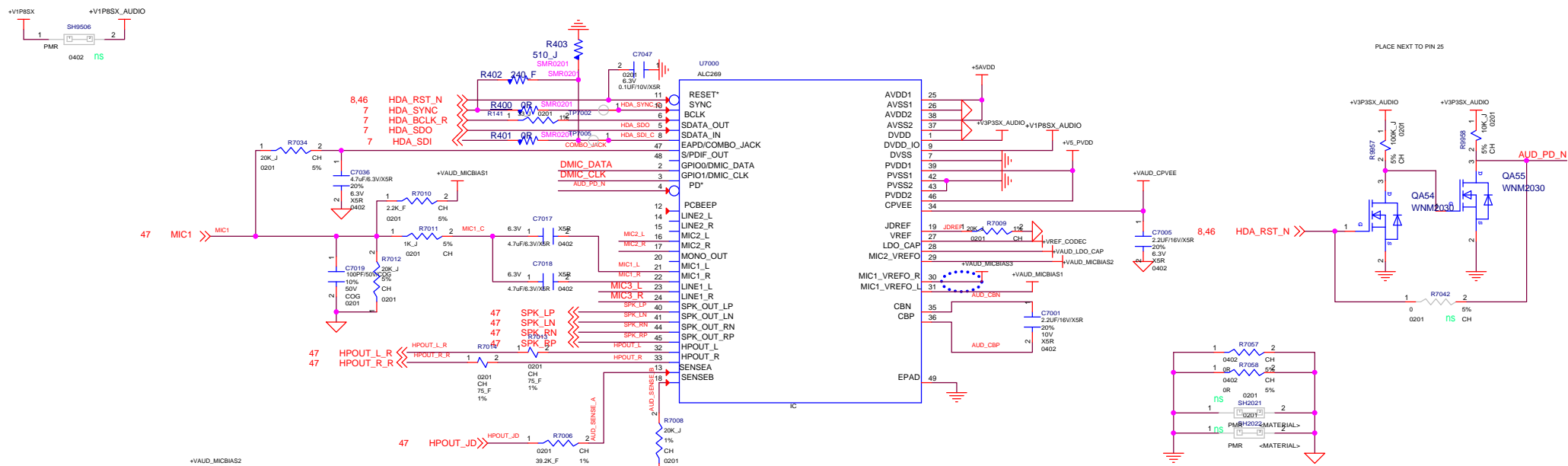
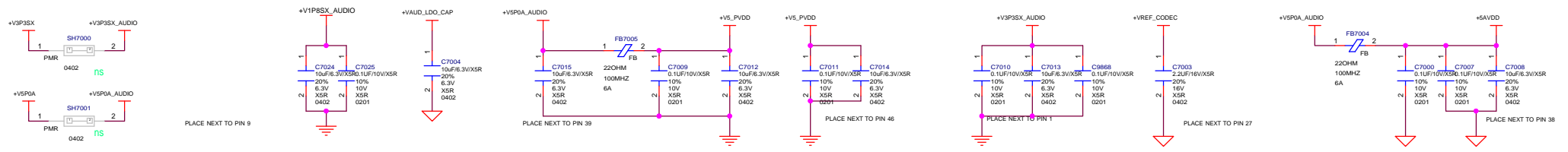




Title		
APOLLO LAKE		
Size	Document Number	Rev
B	WWAN MODULE	R100
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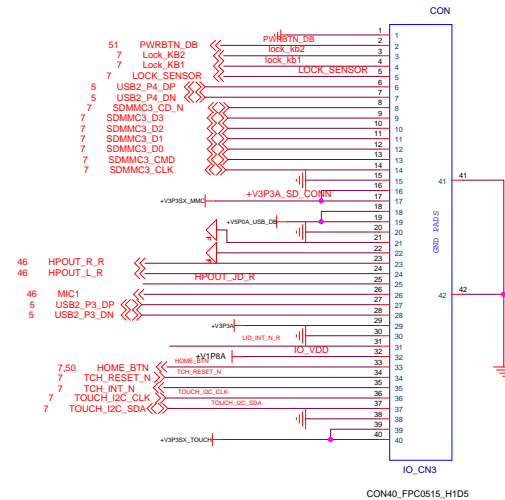
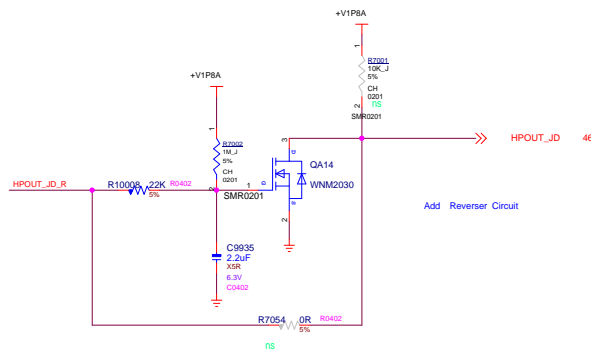
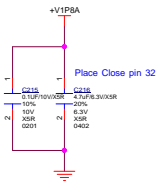
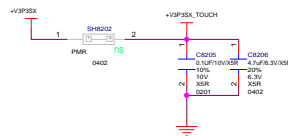
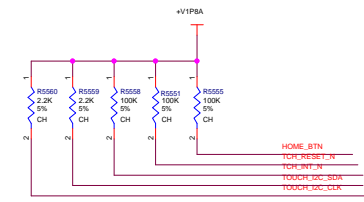
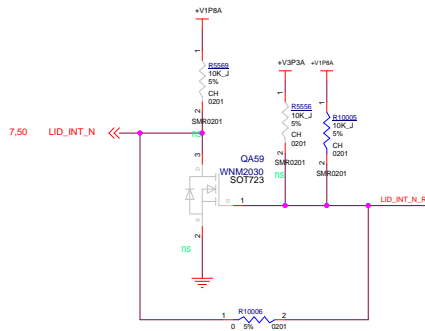
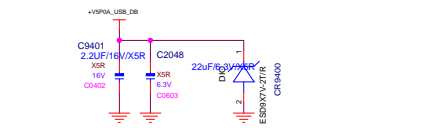
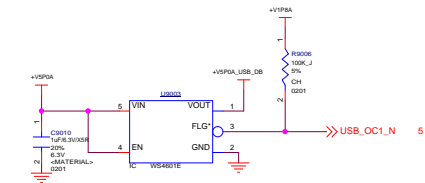
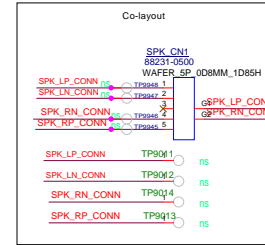
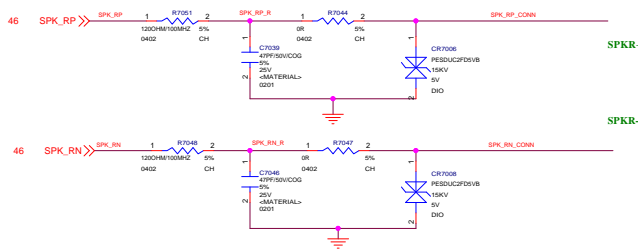
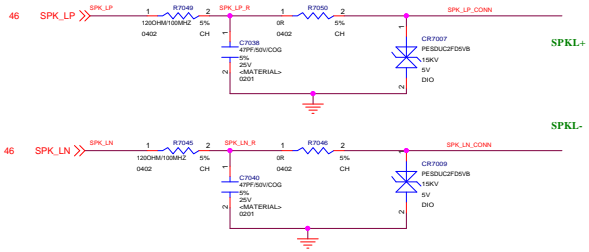


 APOLLO LAKE		
Title APOLLO LAKE		
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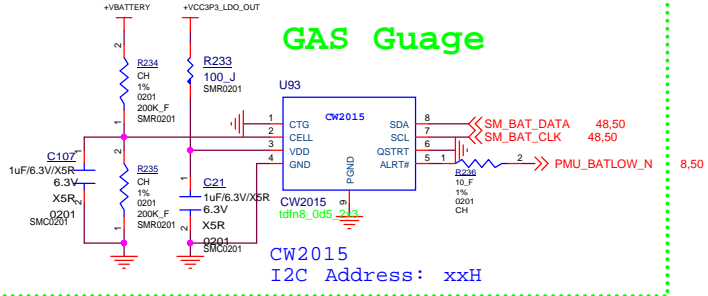


R120 change 2MIC connect to MIC2

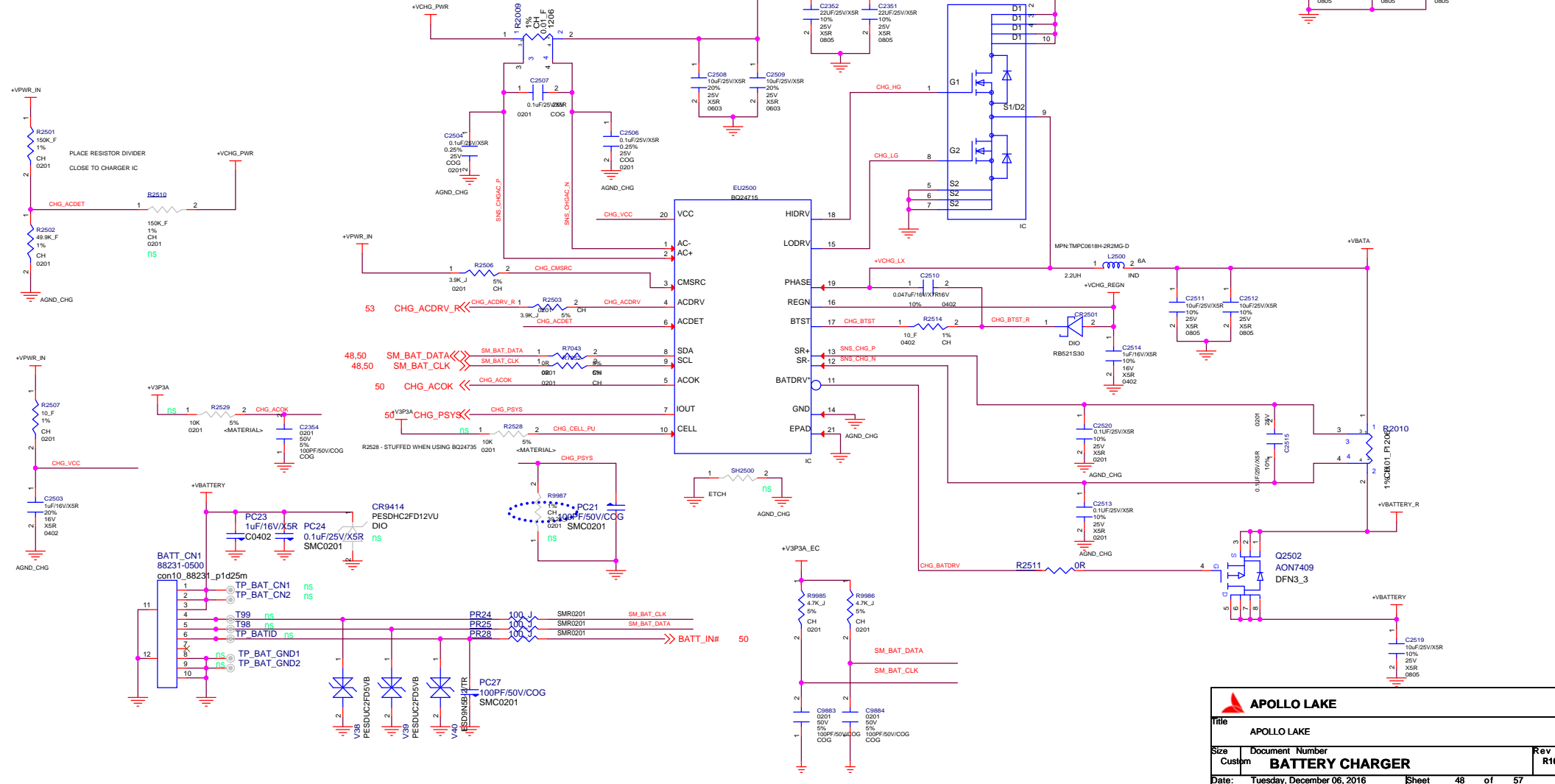
Title APOLLO LAKE		
Size Custom	Document Number AUDIO CODEC	Rev R100
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GAS Guage

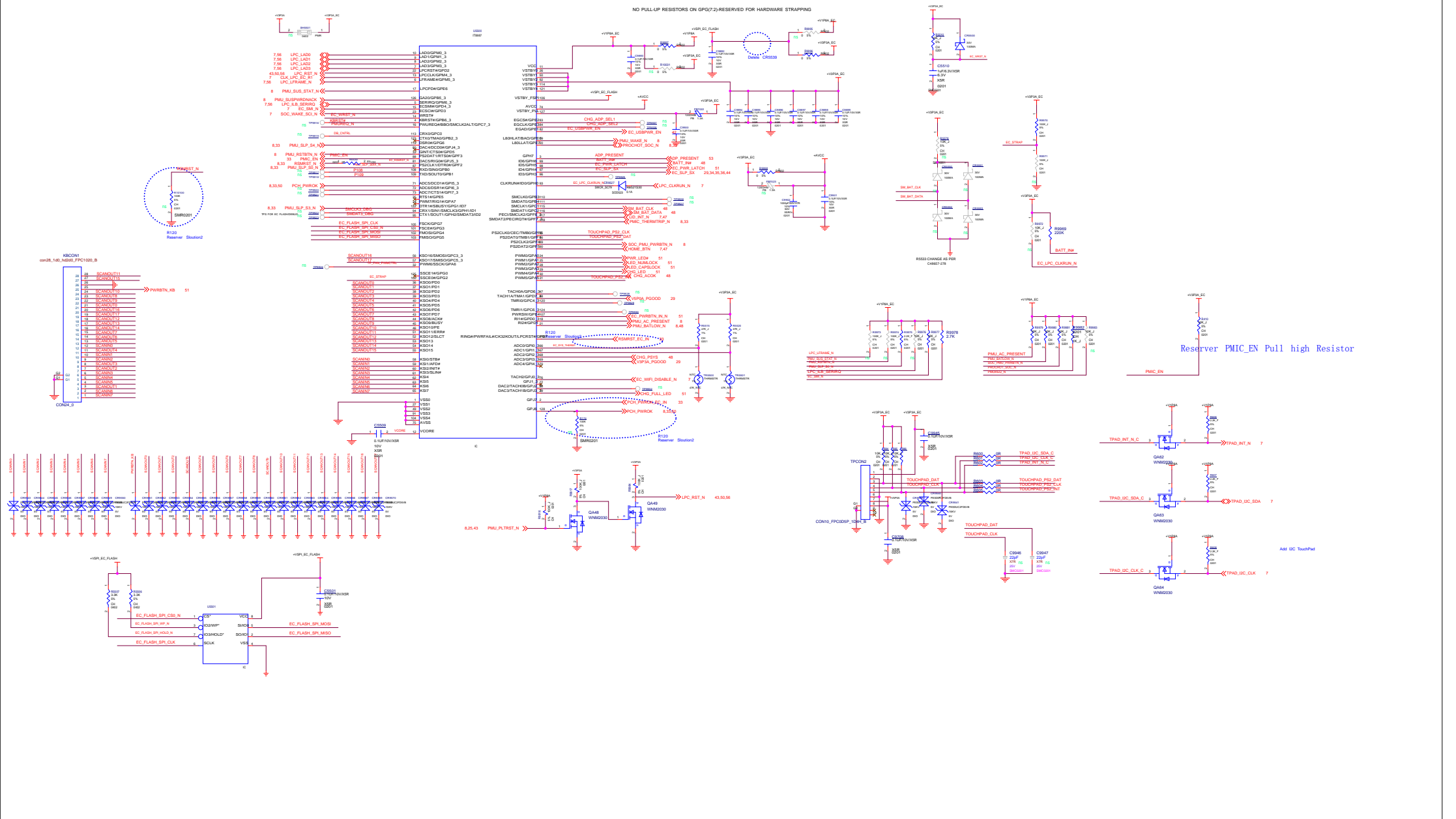


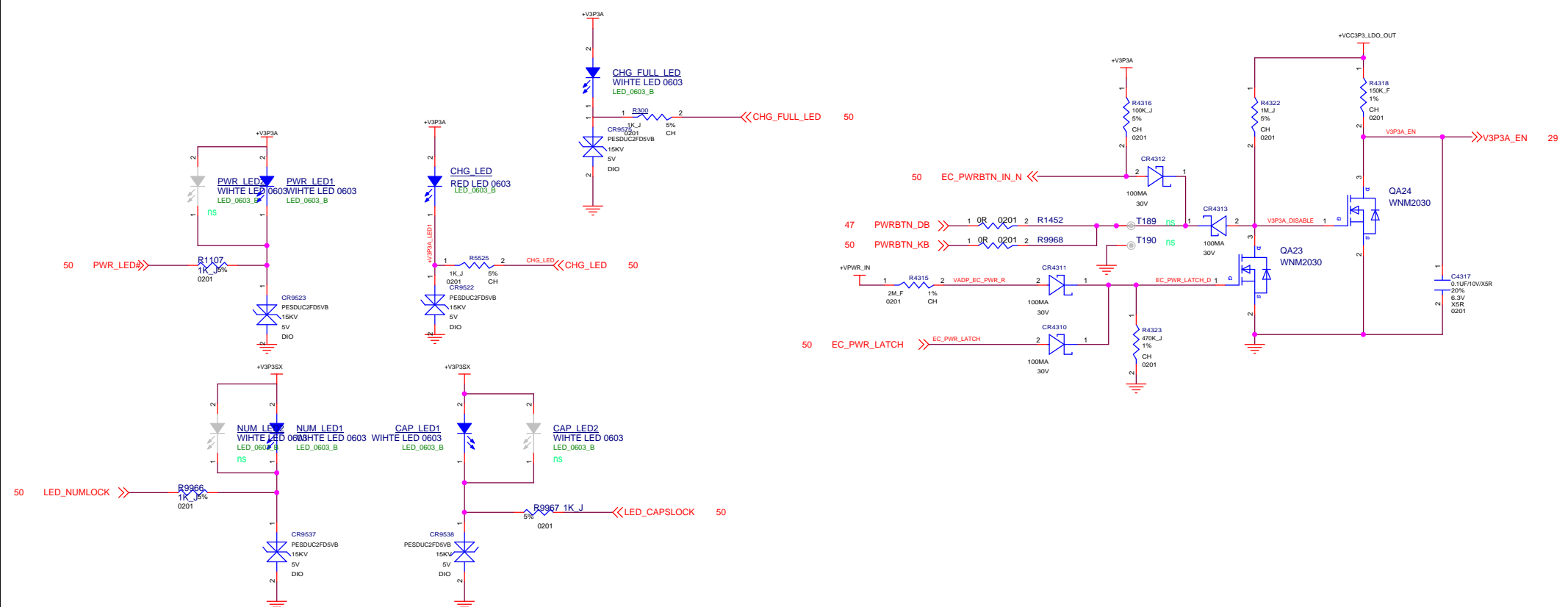
Change SELECT POWER INPUT by Qin 2015.11.11




 APOLLO LAKE		
Title: APOLLO LAKE		
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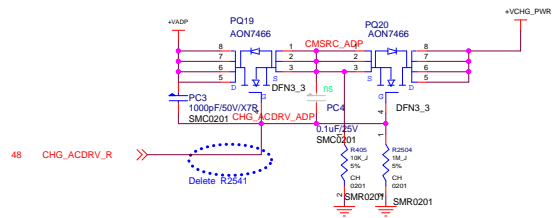
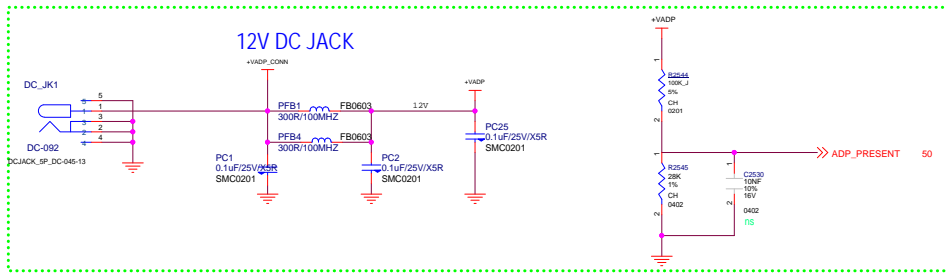
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Title			
APOLLO LAKE			
Size	Document	Number	Rev
B	DC JACK		R100
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Title: APOLLO LAKE		
Size: Custom	Document Number: BUTTONS LEDS AND MISC	Rev: R100
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Title APOLLO LAKE		
Size	Document Number	Rev
Custom	TYPE-C MULTIPLEXER	R100
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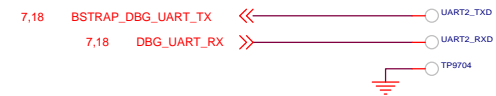
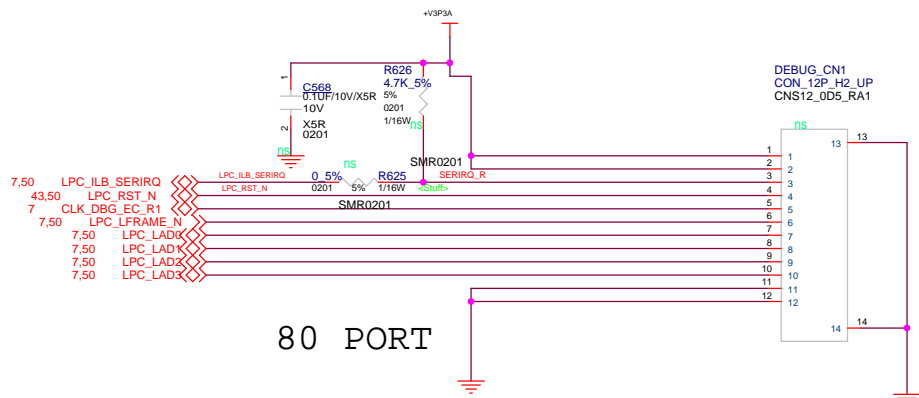


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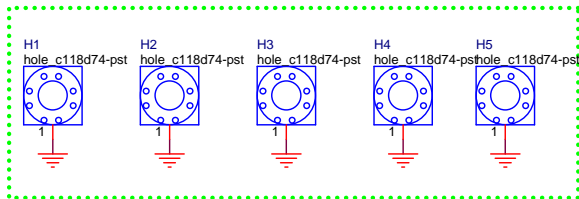
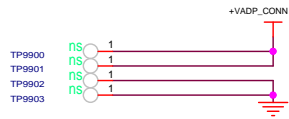
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APOLLO LAKE			
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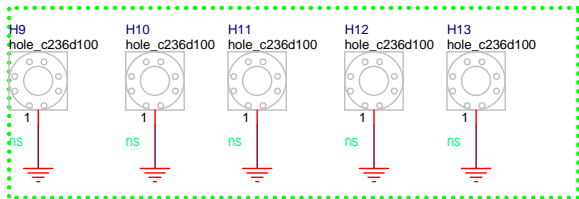
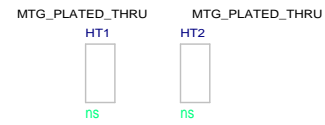
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APOLLO LAKE			
Size	Document	Number	Rev
Custom	TYPE-C CONNECTOR		R100
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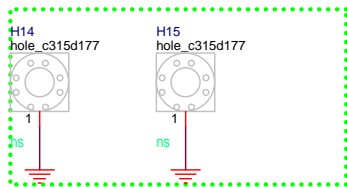
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Size Custom	Document Number DEBUG	Rev R100
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For Thermal



For ME



For ME

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