

# M16QF8 Circuit diagram

REVISION RECORD			
LR	ECO NO.	APPROVED	DATE

D

D

C

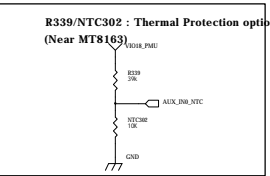
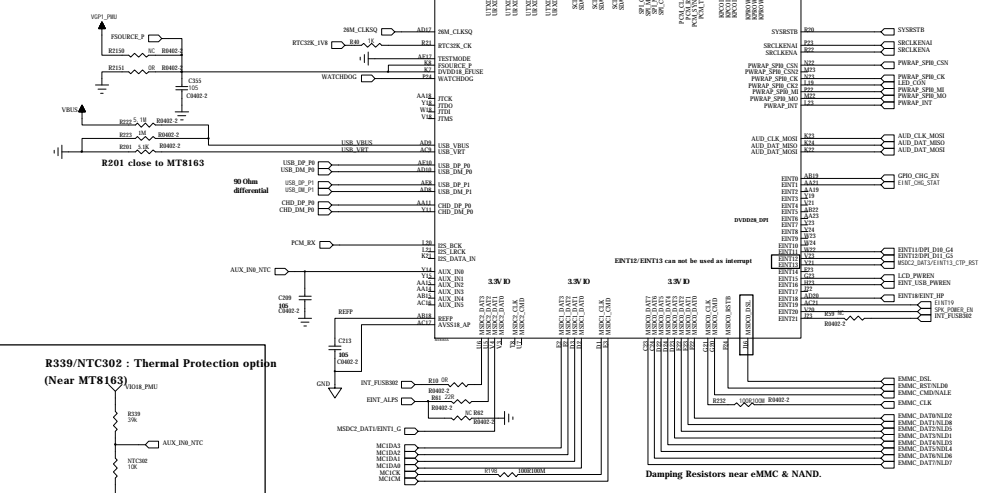
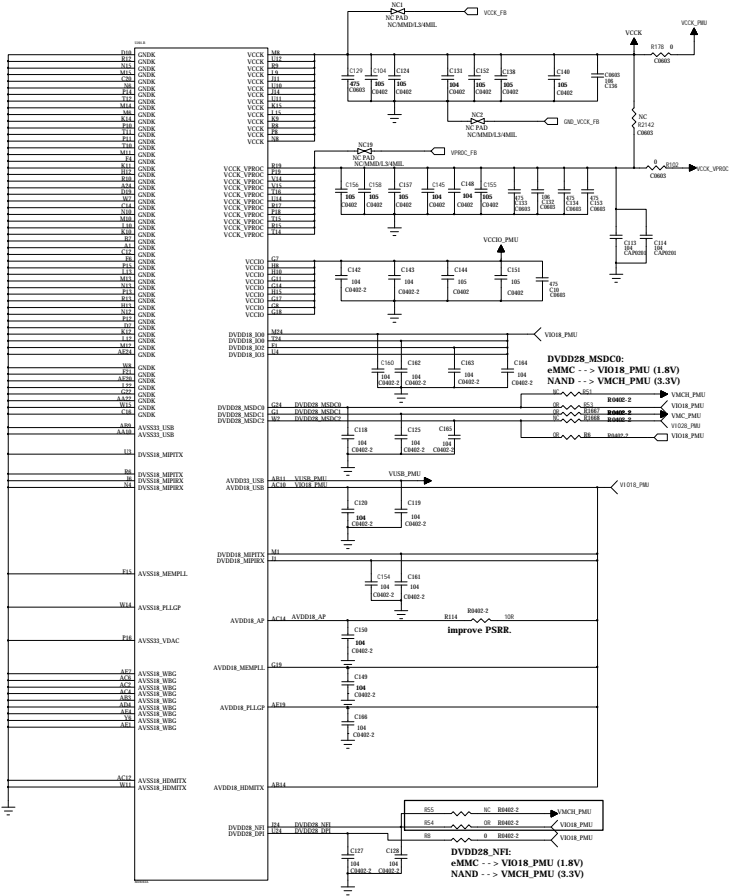
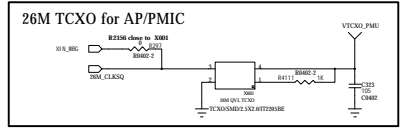
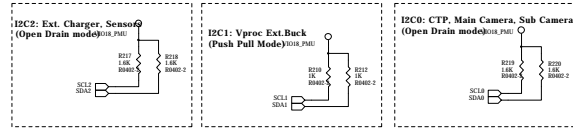
C

B

B

A

A

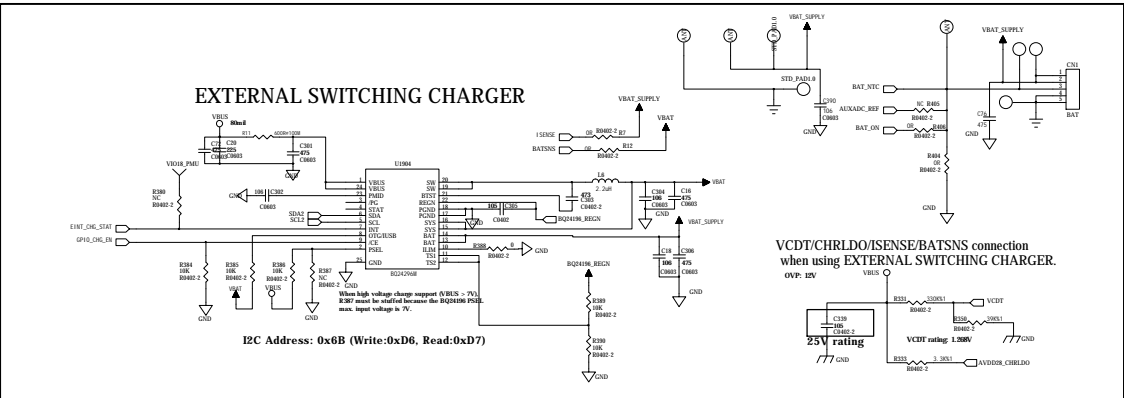
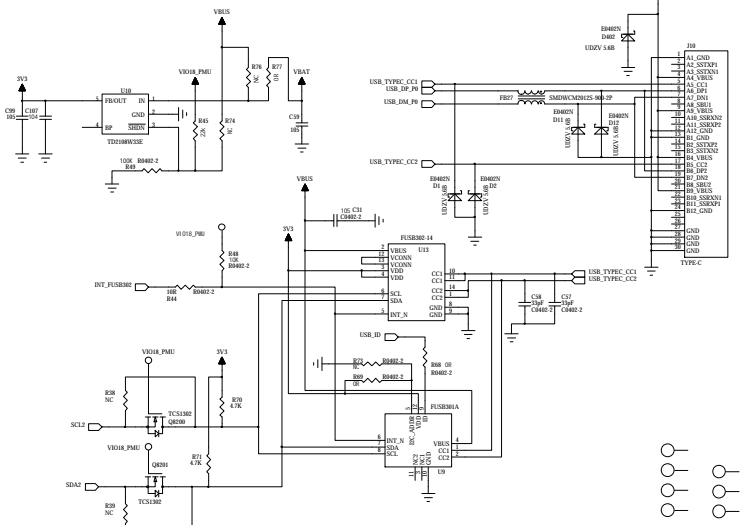
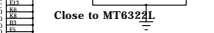
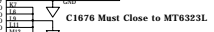
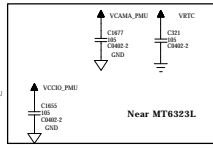
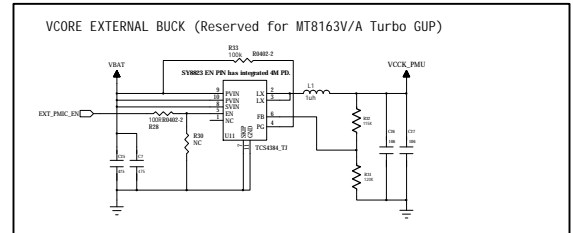
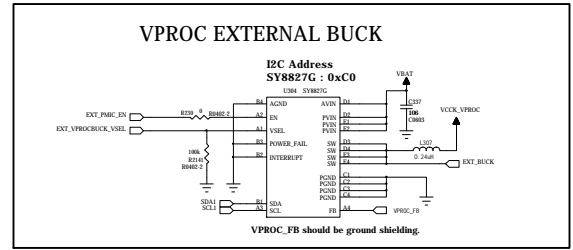
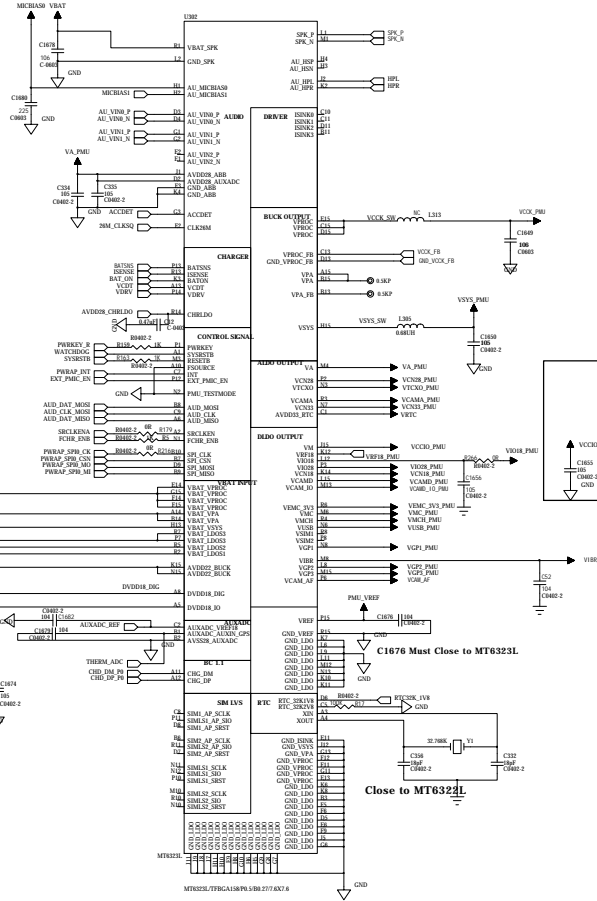


Damping Resistors near eMMC & NAND.

COMPANY		TITLE		7500-M16QF8-01R	
DRAWN	DATE: 2019-03-20	CODE	SIZE	DRAWING NO.	REV.
CHECKED	DATE: 2019-03-20	A1			
QUALITY CONTROL	DATE:	SCALE		SHEET	9
RELEASED	DATE:				

REVISION RECORD			
LTR	ECO NO.	APPROVED	DATE

Symbol	LPDDR2/1.2V	PCDDR3L/1.35V	PCDDR3/1.5V	LPDDR1/1.8V	Default
SPL_CSN	H	L (20K)	H	L (20K)	PU
AUD_MOS	L	H (20K)	L	L	PD

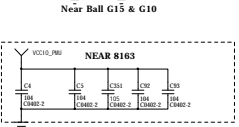
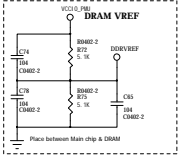
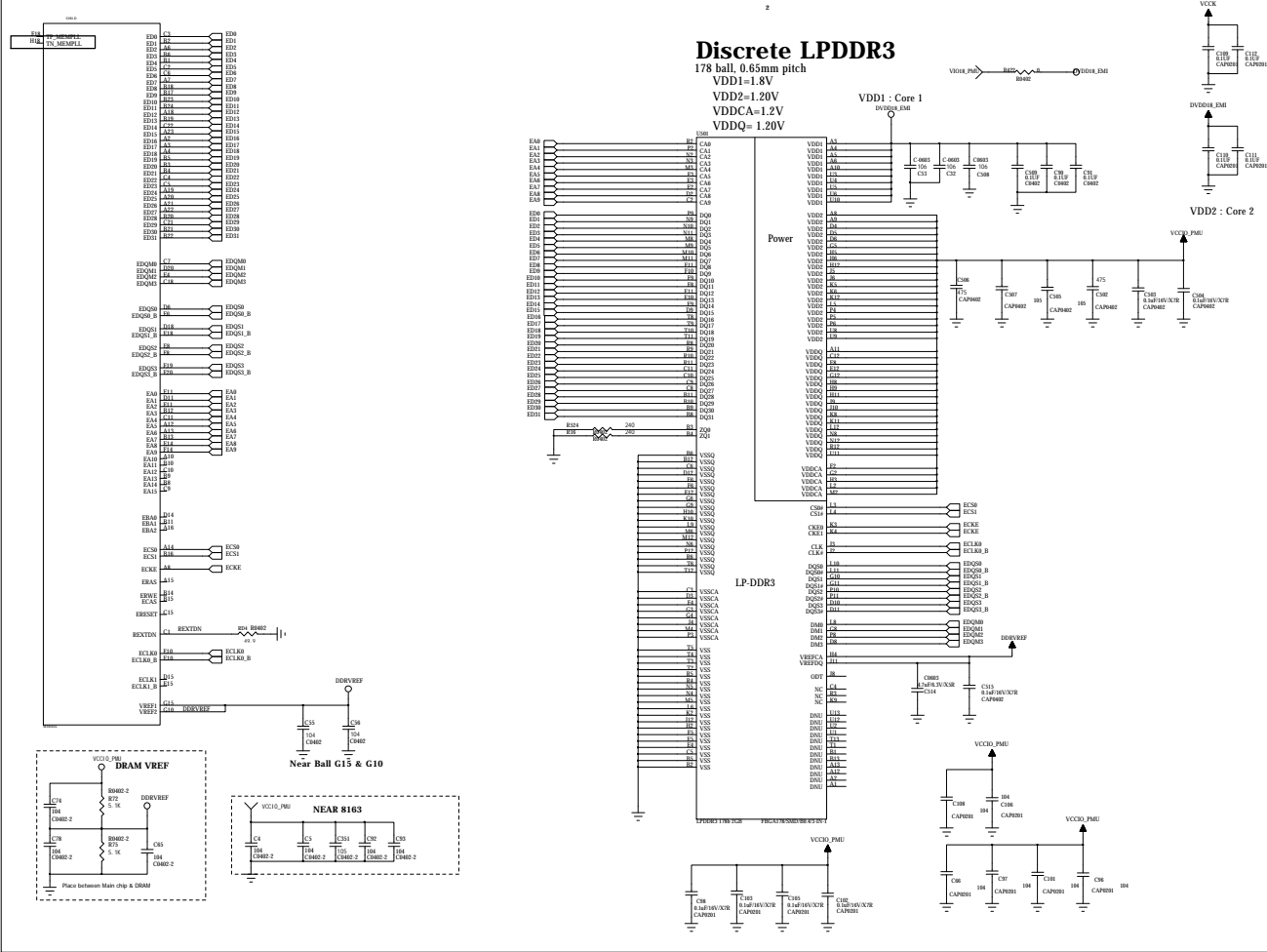


COMPANY		TITLE	
		7500-M16QF8-01R	
DRAWN	DATE: 2019-03-20	CODE	SIZE
CHECKED	DATE: 2019-03-20	DRAWING NO.	REV.
QUALITY CONTROL	DATE:	A1	
RELEASED	DATE:	SCALE	SHEET: 26 9

REVISION RECORD			
LR	ECO NO.	APPROVED	DATE

### Discrete LPDDR3

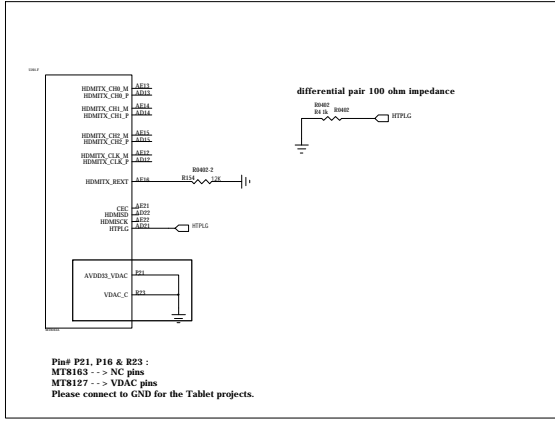
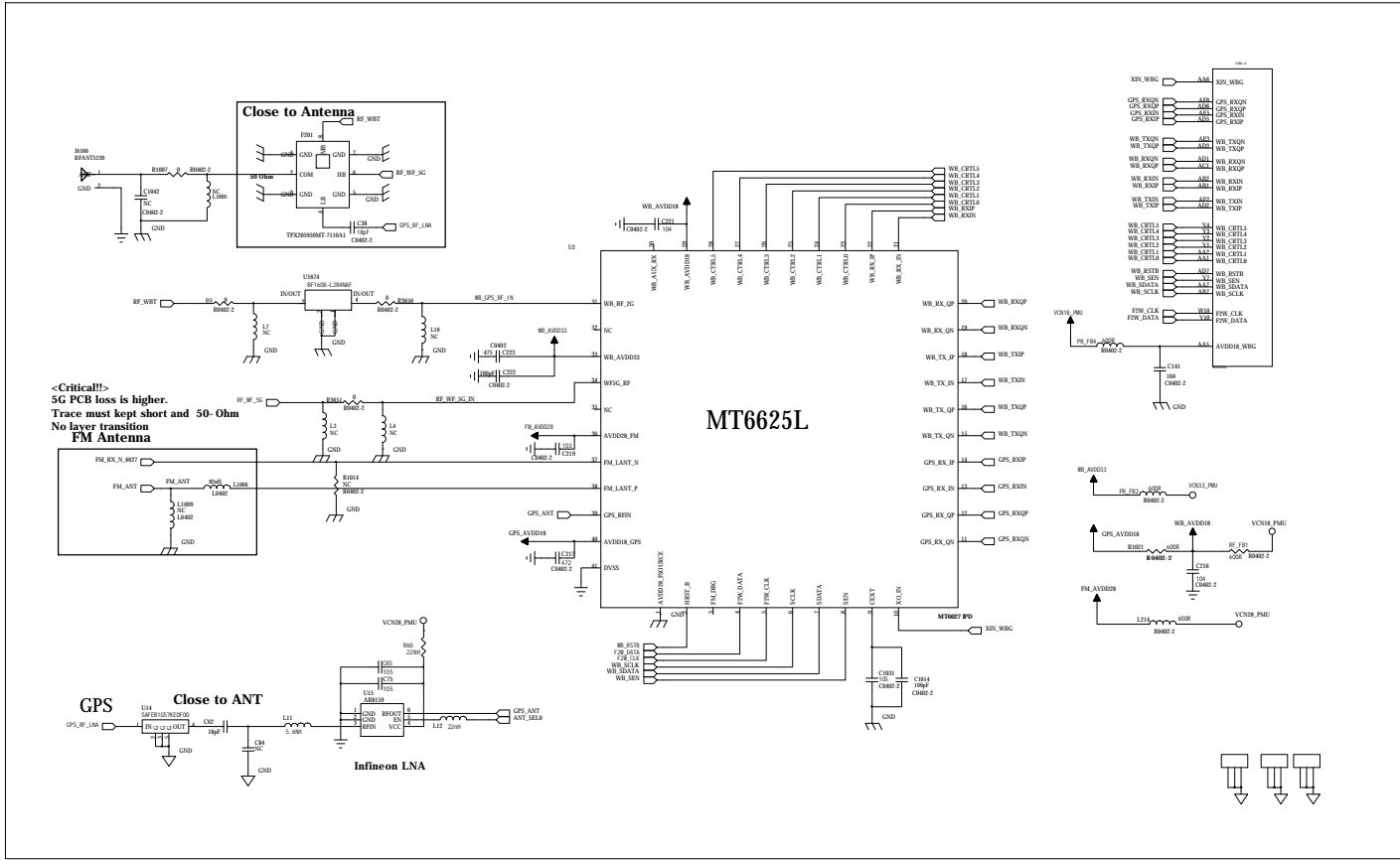
178 ball, 0.65mm pitch  
 VDD1=1.8V  
 VDD2=1.20V  
 VDDCA=1.2V  
 VDDQ= 1.20V



DRAWN	DATE: 2019-03-20
CHECKED	DATE: 2019-03-20
QUALITY CONTROL	DATE:
RELEASED	DATE:

COMPANY:			
TITLE: <b>7500-M16QF8-01R</b>			
CODE:	SIZE:	DRAWING NO.	REV:
<b>A1</b>			
SCALE:	SHEET: <b>34</b>		9

REVISION RECORD			
LR	ECO NO.	APPROVED	DATE

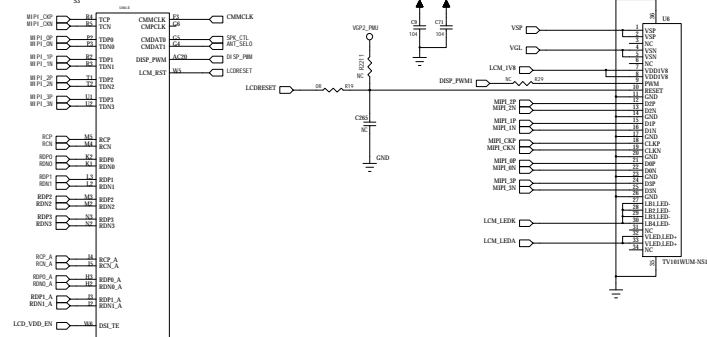


COMPANY		TITLE			
		7500-M160F8-01R			
DRAWN	DATE: 2019-03-20	CODE	SIZE	DRAWING NO.	REV:
CHECKED	DATE: 2019-03-20	A1			
QUALITY CONTROL	DATE:				
RELEASED	DATE:				
SCALE		SHEET: 4# 9			

REVISION RECORD			
TR	ECO NO.	APPROVED	DATE

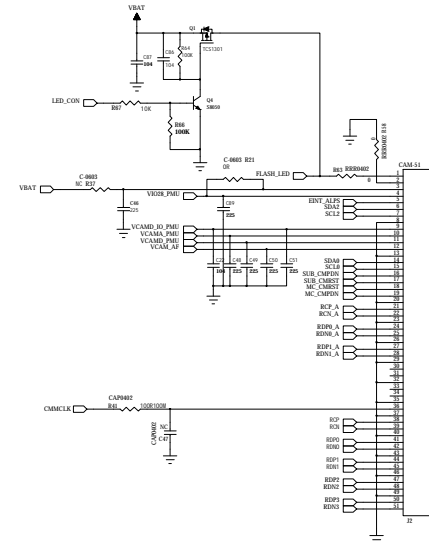
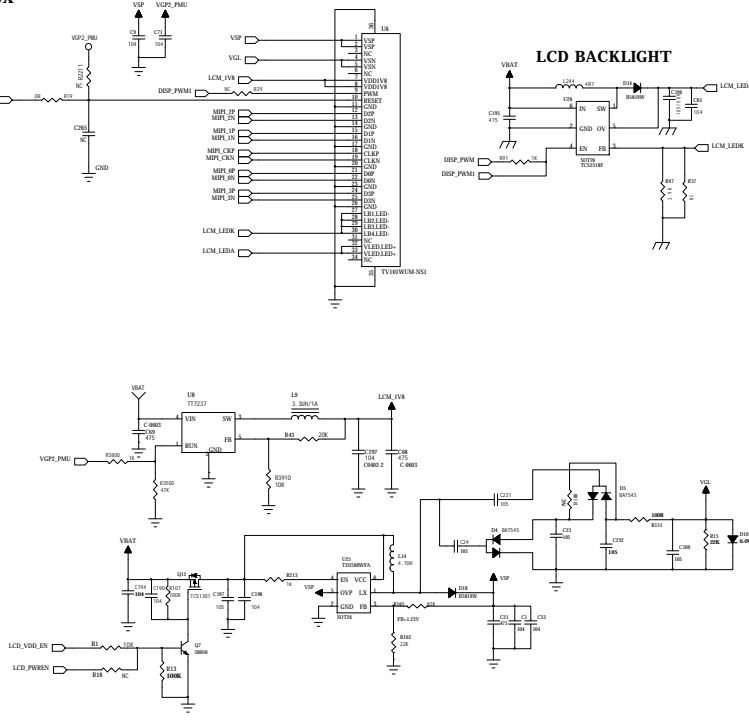
**MT8163 MIPI DSI & LVDS PIN-MUX**

MIPI DSI IF	LVDS IF
TCP	RIN2+
TCN	RIN2-
TDN0	RIN0+
TDN0	RIN0-
TDN1	RIN1+
TDN1	RIN1-
TDN2	CLKIN+
TDN2	CLKIN-
TDN3	RIN3+
TDN3	RIN3-



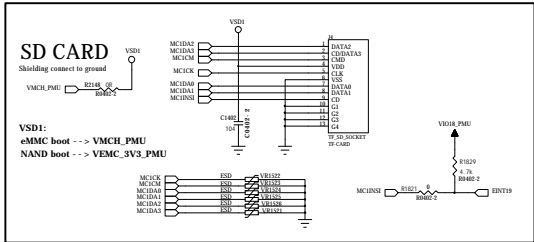
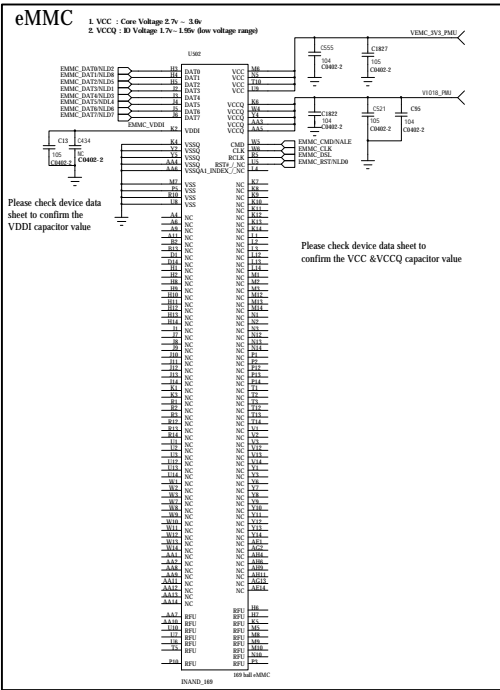
Close to MT8163  
R203 :  
1.5K for MIPI display  
24K for LVDS display

**LCD BACKLIGHT**



COMPANY			
TITLE			
<b>7500-M16QF8-01R</b>			
DRAWN	DATE: 2019-03-20	CODE	SIZE
CHECKED	DATE: 2019-03-20	DRAWING NO.	REV:
QUALITY CONTROL	DATE:	<b>A1</b>	
RELEASED	DATE:		
SCALE		SHEET: 9/9	

REVISION RECORD			
LR	ECO NO.	APPROVED	DATE



D

D

c

c

C

C

B

B

B

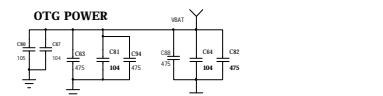
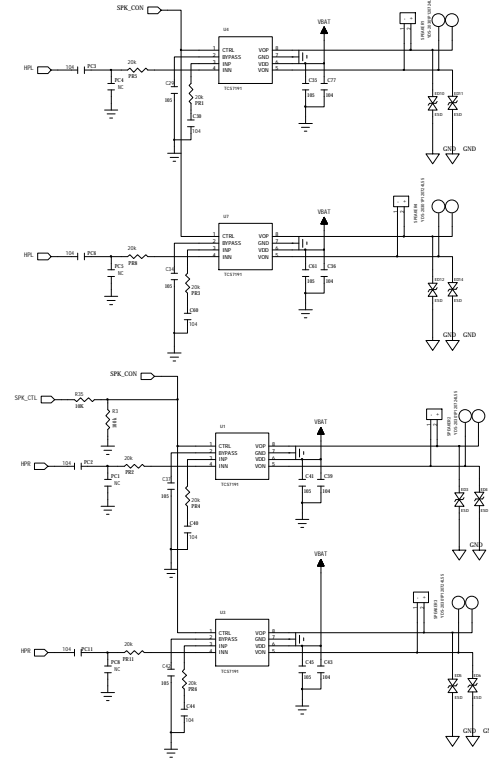
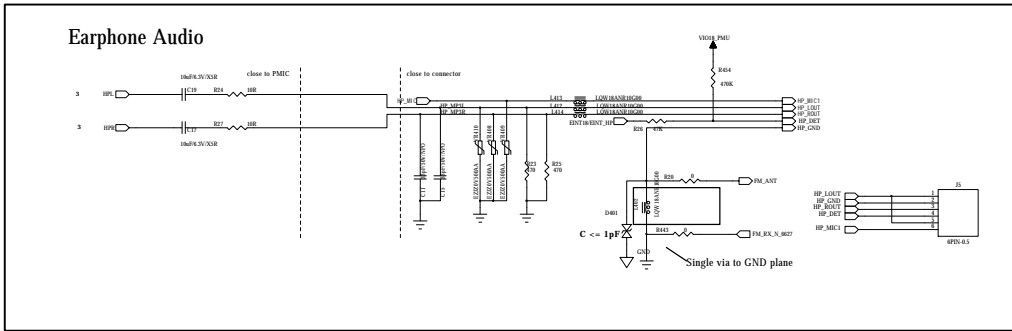
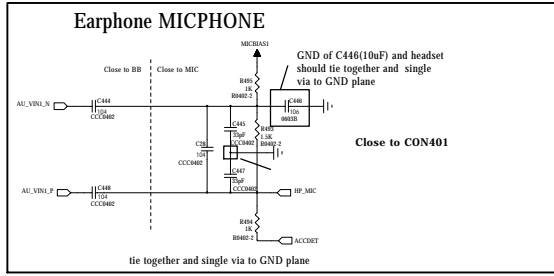
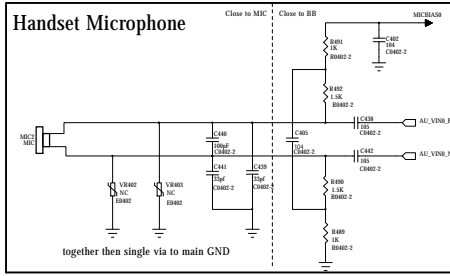
B

A

A

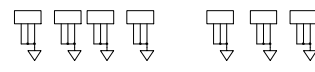
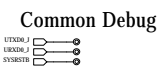
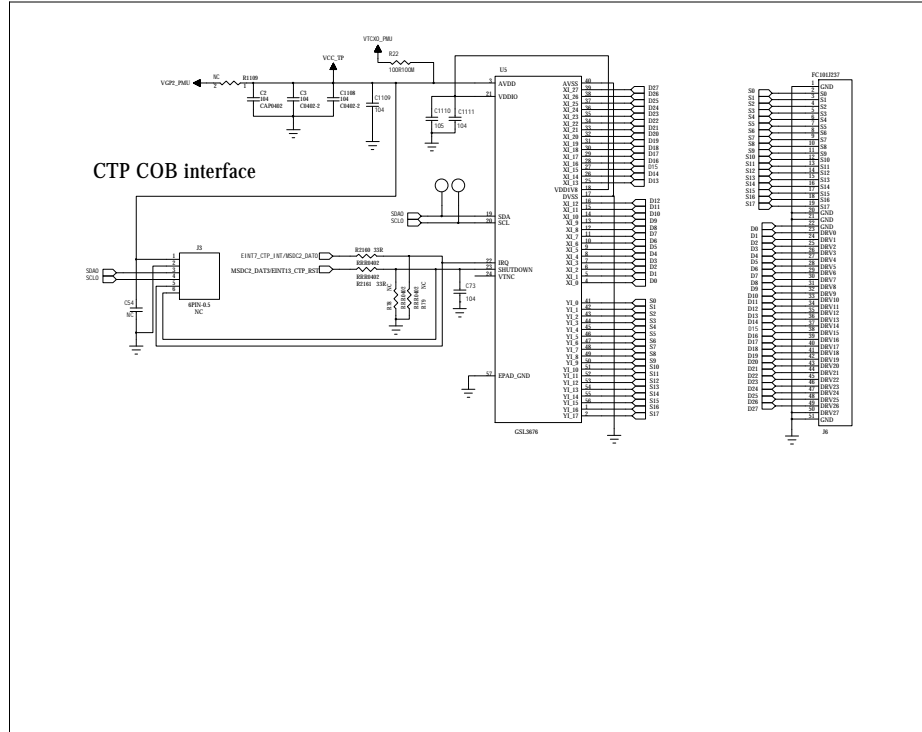
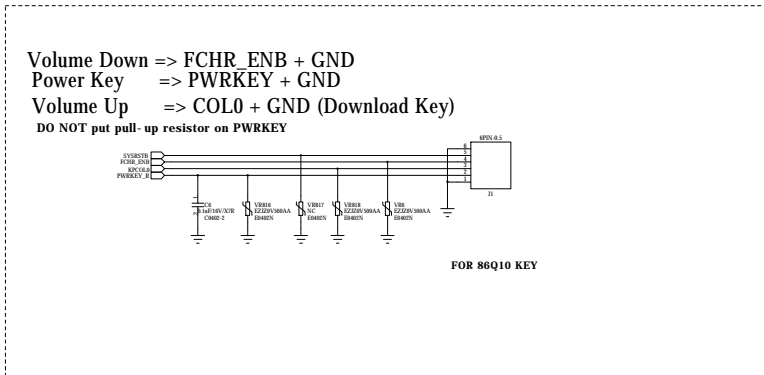
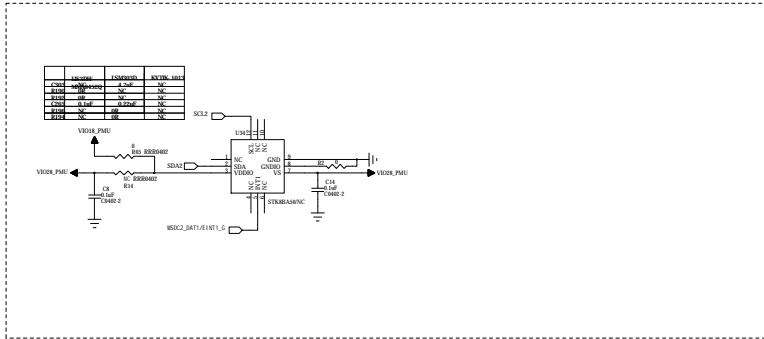
DRAWN:		DATE:		COMPANY:			
CHECKED:		DATE:		TITLE:			
QUALITY CONTROL:		DATE:		7500-M16QF8-01R			
RELEASED:		DATE:		CODE:	SIZE:	DRAWING NO.:	REV.:
				A1			
				SCALE:		SHEET: 8/9	

REVISION RECORD			
LT#	ECO NO.	APPROVED:	DATE:



COMPANY:			
TITLE:			
7500-M160F8-01R			
DRAWN:	DATE:	CODE:	SIZE:
	2019-03-20		
CHECKED:	DATE:	DRAWING NO.:	REV.:
	2019-03-20		
QUALITY CONTROL:	DATE:	A1	
RELEASED:	DATE:	SCALE:	SHEET: 7# 9

REVISION RECORD			
LT#	ECO NO.	APPROVED	DATE



DRAWN:		DATE:		COMPANY:			
CHECKED:		DATE:		TITLE:			
QUALITY CONTROL:		DATE:		7500-M16QF8-01R			
RELEASED:		DATE:		CODE:	SIZE:	DRAWING NO.:	REV.:
				A1			
				SCALE:		SHEET: 9/9	



REVISION RECORD			
LT#	ECO NO.	APPROVED:	DATE:

Version	
<b>V01</b>	<b>First Release.</b>
<b>V02</b>	<b>1. L309 change to NC.</b>
<b>V03</b>	<b>1. Fix the CS0# link error at U5 pin# L2. 2. Add C213 notice for MT8163 &amp; MT8127 REFP value selection. 3. Add RD4 notice for MT8163 &amp; MT8127 REXTDN value selection.</b>
<b>V04</b>	<b>1. Delete C210, R371, NTC301. (Reserve for Battery NTC) (P2 &amp; P3) 2. Change U304 PN from SYM827 to SY8827G. (P4) 3. Update R2140 &amp; C337 circuit to reserve the VBAT LC input to reduce the noise .</b>

D

D

C

C

B

B

A

A

DRAWN:		DATE: 2019-03-20		COMPANY:			
CHECKED:		DATE: 2019-03-20		TITLE: 7500-M160F8-01R			
QUALITY CONTROL:		DATE:		CODE:	SIZE: A1	DRAWING NO.:	REV.:
RELEASED:		DATE:		SCALE:		SHEET: 9# 9	